ATLAS ITk Electronics Specification: ABCStarV1

Version: 1.0

August 13, 2021

Abstract

The ABCStar chip will be the front-end ASIC for the readout of the ITK Silicon Strips detector in the ATLAS experiment for the HL_LHC collider at CERN.

Revision History

Revision	Date	Author(s)	Description
1.0	5 Jan 2021	P. Leitao, J. J. John, J. Kaplon	Initial draft. Content is heavily based on ABCStarV0 specifications by F. Anghinolfi, P. Keener, M. Newcomer, B. Gallop, M. Warren, H. Grabas, J. Kaplon, J. J. John and P. Leitao
1.1	13 Aug 2021	P. Leitao	Fixed typo in the documentation

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1 Conventions and Glossary

1.1 Conventions

Signal names ending with the letter 'b' are active low, all other signals are active high, unless otherwise noted.

Hexadecimal numbers are noted by prepending $, or "0x" or using Verilog notation: <number of bits>'h<hexadecimal value>, eg (32'h0123beef). All values are MSB (most signification bit first) unless other wise expressed.

Note: LP was formerly called L1, and PR was formerly called R3, in past documentations (as for ABC130).

1.2 Glossary

BC — Bunch Crossing Clock from the accelerator, at 40 MHz.

BCID — Bunch Counter ID. An 8-bit clock counter used to detect front-end desynchronization.

BCR — Bunch Counter Reset. A 1-bit BC-synchronous command that resets the BCID to zero. It is used to ensure front-end synchronization. It is issued through the LCB input.

CMD — Command signal. Used for asynchronous setup of the HCCStar and ABCStar or for performing certain resets.

Command Sequence — A set of LCB command frames starting with a Start of Sequence frame and ending with an End of Sequence frame that together make up a single command. The frames in a Command Sequence must be in order, but need not be consecutive.

HPR — High Priority Register. A special register that contains ABCStar status information. It is sent at least once after reset. By default, it is send 500 us after lock acquisition, and if not disabled, every ms after the first HPR. An HPR is also issued at LCB link status change.

L0A — Level 0 Accept. A beam crossing synchronous pulse that, together with L0tag[6:0], transfers strips data from the fixed latency pipeline on the ABCStar (known as L0Buffer) to the EventBuffer to the address specified by L0tag[6:0]. An L0A does not generate an ABCStar readout.

L0tag — A 7-bit value attached to each L0A. It is used to safely identify events for readout.

LCB — L0A/CMD/BCR signal.

LP — Low Priority readout request. An asynchronous request from the HCCStar to the ABCStar to read out an event with the given L0tag from the ABCStar event buffer with low priority.

PR — Priority readout request. An asynchronous request from the HCCStar to the ABCStar to read out an event with the given L0tag from the ABCStar event buffer with high priority. Generated on the HCCStar by an R3 request.

lsb — Least Significant Bit. This is the bit in the 2^0 place.

msb — Most Significant Bit. This is the bit with the most value in the word.

RCLK — Readout Clock. A 160 MHz clock from the HCCStar used to decode the LCB signal on the ABCStar and to clock the serial output bit stream from the ABCStar back to the

HCCStar.

SEE — Single Event Effect. Any of a number of effects induced by radiation, electromagnetic interference, or other causes that may make change the stored stated or behavior of a circuit. Single Event Upset (SEU) and Single Event Transients (SET) are two types of SEE.

TID — Total Ionizing Done.

2 Related Documents

"ATLAS ITk Strip System Architecture", EDMS AT2-IS-ER-0001,
https://edms.cern.ch/document/AT2-IS-ER-0001

Please also see table 6.1

3 Description of Component or Facility

The ABCStar ASIC must provide all functions required for processing of signals from 256 strips of a silicon strip detector in the ATLAS experiment employing a binary readout. The architecture chosen for the ABCStar allows a multi-trigger data flow control retaining the Beam Crossing synchronous pipeline transfer signal (L0 here) from previous versions, an asynchronous Regional Readout Request (PR here) and a second level asynchronous data readout intended for a global readout (LP here). The design can be easily adapted to a single level readout (L0 readout mode) simply by not sending priority triggers. The simplified block diagram of the chip is shown in figure 3.1. The main functional blocks are: front-end including threshold and calibration controls, power regulation, command decoder, Mask and Edge Detection, L0Buffer, EvtBuffer, Cluster Finder and Readout logic. The "Top_Logic" block controls the data path by handling all the incoming requests, such as PR, LP and register reads, and assigning a prioritization scheme for the readout packets.

The front-end is optimized for 2.5cm strips (but can be up to 5cm strips) with 25ns shaping time, and a noise level below 1000 electrons after full radiation effects. The discrimination level should be lower than 1 fC, possibly reaching 0.5 fC. After discrimination, at each bunch crossing the binary outputs of the front-end channels are sampled and stored into the L0Buffer for a duration fixed by the (programmable) latency for receiving the L0 signal.

At each L0 reception the event with the correct latency is transferred from the EvtBuffer to the location specified by the L0tag[6:0] value, or in another words, the event is tagged with the L0tag[6:0]. It is maintained until overwritten by another L0 with the same L0tag[6:0] (only 128 values are possible). If a PR or LP signals are received with the corresponding L0tag number, the event is copied from the EvntBuffer and processed through the Cluster Finder (CF). The CF block acts as a data reduction circuit, creating a "cluster" byte for channels found with hits. The expected average occupancy is of 2 (4 in case of 5cm strips) clusters per event. The Readout block generates formatted packets with the event identification and the associated cluster bytes. The data is transmitted serially at 160 Mb/s.

The LCB Decoder block decodes the LCB protocol from the LCB_IN signal at 160 Mbps. It is possible to send L0 trigger signals (L0 and L0tag), fast command resets (eg, BCR) and to have access to the configuration registers for read and write purposes.

The PRLP input receives the LP and PR trigger signals. The Top Logic block is the autonomous sequencer that controls the data flow path according to the arrival of the L0, register accesses, PR and LP trigger signals.

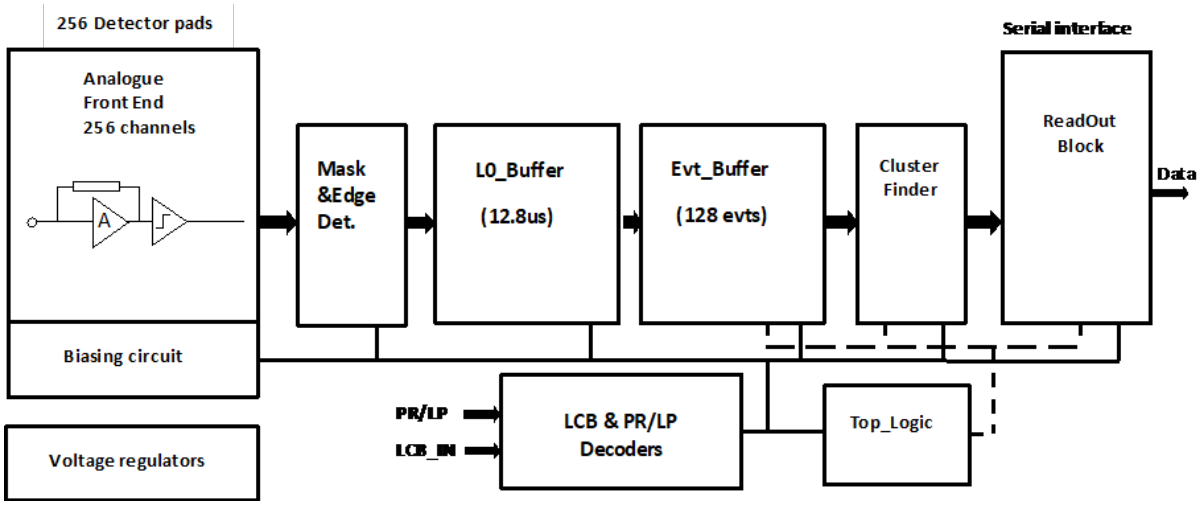

Figure 3.1: Block diagram of the ABCStar chip

4 Modifications from the prototype ABCStarV0

A summary of the main changes between the ABCStarV0 (May 2018 prototype) and ABCStarV1 are presented below:

- **Die Size** The die size has changed due to reticule constraints. Refer to table 4.1
- **Pad Details** The ABCStarV1 has the same padring as the ABCStarV0. It has the same number and size of pads, located at the same co-ordinates/positions. However, the meaning and directionality of some of those pads has changed:
  - DAT and DATB has been swapped: DAT differential pad has now inverted polarity with regards to ABCSTARV0
  - JTAG pads have been repurposed:
    - Input JTAG pads physically exist BUT are not connected (the i/o cell is exactly the same)
    - Output JTAG pads were repurposed:
      - Scan_Enable is now unused
      - SDI_CLK is now unused
      - SDI_BC is now unused
      - SDO_CLK is now TESTOUTPUT
      - SDO_BC is now TESTOUTPUTB
- **Analog core changes** No changes in the analog FE
- **Digital Core changes**
  - The design has been fully triplicated using triple voters, triple logic and triple clocks. All asynchronous resets have changed to synchronous (apart from configuration logic). A reset synchronizer (async set and sync release) has been also been added.
  - The packet header and contents have slightly changed.

- shunt_ctrl block has been removed but shunt still exists: this change reduces the digital current consumption during the TID bump to give room to the additional triplication logic.
- Register map was optimized.
- A possibility to gate the triplicated clocks has been added.
- A way to reset the ADC has been added. By default the ADC is disabled. It is recommended to issue a reset after enabling the ADC.
- LCB_SelfResetEnable feature: This was added as a backdoor to the LCB decoder. This self resets the LCB decoder when the LCB decoder error reaches saturation defined in register LCB_ErrCount_Thr[7:0].
- A ring oscillator has been added for the digital logic radiation degradation monitoring.
- Triplicated glitch filters have been added to the configuration pads (eg, RSTB, padID, etc) and to the BC clock (40 MHz). No glitch filtering has been added to RCLK (160 MHz).
- An idle pattern has been added to the serializer output. This is to help HCCStar during deserialization.
- The flag bit in the packet status bits has been redefined.
- Digital LDO regulator coding has been changed from binary to decimal.
- Analog LDO regulator encoding has been changed from binary to decimal.
- The BTMUX (analog mux) encoding is now decimal.
- A fixed rotary pattern with the BCID counter has been added. This produced expected packets in order to help determine the radiation crosssection.
- Added a timer to the readout block to prevent stuck states.
- Added a configuration bit to refer packet format to ABCStarV0.
- An SEU counter (8-bits) has been added. It increases with when a voting action occurs in the ADCS registers.
- Fusing address selection encoding has changed from binary to decimal.
- A digital test output mux has been added. Its output can be found in TESTOUTPUT and TESTOUTPUTB. The outputs are **CMOS outputs and not differential** although TESTOUTPUTB is the inverted signal of TESTOUTPUT. Do not connect a termination resistor between TESTOUTPUT and TESTOUTPUTB.
- All FIFOS have been downsized to save logic:
  - PR fifo: depth of 4
  - LP fifo: depth of 4
  - REG fifo: depth of 4
  - Cluster finder fifo: depth of 4
  - HPR fifo: depth of 2
  - L0Buffer fifo: depth of 1

	Long-edge (LE)	Short-edge (SE)	V1's LE wrt V0	V1's SE wrt V0
ABCStarV0	8.087 mm	7.120 mm	-	-
ABCStarV1	8.087 mm	7.150 mm	0.000 mm	0.03 mm

Table 4.1: ABStarV0 and ABCStarV1 die size comparison

5 Known Issues

- **SEU Counter** The "SEU" signal going to the counter is not synchronized to the 40 MHz clock. This can break the SEU Counter which has been seen during SEE testing.

6 Interfaces

This component uses and interfaces with other components listed in Table 6.1.

Name of Component	**Name of Component Specification**
HCCStar ASIC	HCCStar Specification [1]
AMAC ASIC	AMAC Specification [2]
Barrel and Endcap Hybrid Boards	Hybrid Board Specification [5]
Barrel and Endcap Power Boards	Power Board Specification [7]
Barrel and Endcap Modules	Module Specification [6]
Barrel and Endcap Bus Tapes	Bus Tape Specification [3]
End of Substructure Card	EOS Specification [4]

Table 6.1: Components which interface to this component.

7 Physical Description

The ABCStarV1 has a chipring of 7.9 mm $\times$ 7.0 mm. The physical die dimensions after dicing are 8.087 mm $\times$ 7.150 mm.

The chipring is 7.9 mm wide to fit at best the input pads of the sensor strip pitch, while keeping a reasonable gap between adjacent chips to allow the placement of decoupling capacitors. The pads to the detector are 62 x 200 um with a pitch of 119 um horizontally and 150 um vertically. They are arranged in 4 rows of 64 pads, and for the detector reference GND (HV decoupling and guardring) there are 4 pads on each side of the staggered input pads. The "digital and power" pads are 95 x 190 um. For reference 7.2.

The floorplan for ABCStarV1 is shown in Figure 7.1 and the pad list is shown in Table 7.1.

The pads on both left and right side are to be used during fusing and wafer probing and should not be connected on the hybrids. The VFUSE pad on "bottom" side has to be connected to DVDD (VDD raw) on the hybrids to ensure proper bias of the efuses block.

	rate (MHz)	direction	Type		DC
from the detector (front)					
AIN[255:0]	–	I	Analogue	Inputs to FE channels	
Left side signals					
DVSS		Power	ESD Return	0V Ground specific to ESD return	0V
VFUSE		Power	Efuse Power	To VDD raw on hybrid	3.3/1.5V
FusePP_pad		I	CMOS Pull-Down	To efuse units	0V

"Back" side signals					
DVSS		Power	ESD Return	0V Ground specific to ESD return	0V
VFUSE		Power	Efuse Power	To VDD raw on hybrid	3.3/1.5V
BC_padN	40	I	SLVS	40MHz clock input	
BC_padP	40	I	SLVS	40MHz clock input	
DVSS		Power	ESD Return	0V Ground specific to ESD return	0V
PRLP_padN	40 DDR	I	SLVS	Multiplexed PR LP input (80Mb/s)	
PRLP_padP	40 DDR	I	SLVS	Multiplexed PR LP input (80Mb/s)	
GNDD		Power	Digital Ground	0V Digital Ground	0V
RSTB_Pad	Static	I	CMOS Pull-Up	External Hard Reset signal	1.5V
PowerLow_pad	Static	I	CMOS Pull-Down	Low Power mode when at one	0
GNDD		Power	Digital Ground	0V Digital Ground	0V
padShuntCtrl	Analogue	I	Analogue	Shunt Device Control (analogue signal)	
GNDD		Power	Digital Ground	0V Digital Ground	0V
DVDD		Power	Ext. Digital Power	Ext. Power for Digital	1.5V
VDDD		Power	Reg. Digital Power	Regulated Power for Digital	1.2V
GNDD		Power	Digital Ground	0V Digital Ground	0V
DVDD		Power	Ext. Digital Power	Ext. Power for Digital	1.5V
VDDD		Power	Reg. Digital Power	Regulated Power for Digital	1.2V
GNDD		Power	Digital Ground	0V Digital Ground	0V
DVDD		Power	Ext. Digital Power	Ext. Power for Digital	1.5V
VDDD		Power	Reg. Digital Power	Regulated Power for Digital	1.2V
DVSS		Power	ESD Return	0V Ground specific to ESD return	0V
AVSS		Power	ESD Return	0V Ground specific to ESD return	0V
GNDIT		Power	Analogue Ground	0V Analogue Ground to FE branch	0V
VDDA		Power	Reg. Analogue Power	Regulated Power for Analogue	1.2V
GNDA		Power	Analogue Ground	0V Analogue Ground	0V
AVDD		Power	Ext. Analogue Power	Ext. Power for Analogue	1.5V
GNDIT		Power	Analogue Ground	0V Analogue Ground to FE branch	0V
VDDA		Power	Reg. Analogue Power	Regulated Power for Analogue	1.2V
GNDA		Power	Analogue Ground	0V Analogue Ground	0V
AVDD		Power	Ext. Analogue Power	Ext. Power for Analogue	1.5V
GNDIT		Power	Analogue Ground	0V Analogue Ground to FE branch	0V
VDDA		Power	Reg. Analogue Power	Regulated Power for Analogue	1.2V
GNDA		Power	Analogue Ground	0V Analogue Ground	0V
AVDD		Power	Ext. Analogue Power	Ext. Power for Analogue	1.5V
GNDIT		Power	Analogue Ground	0V Analogue Ground to FE branch	0V
VDDA		Power	Reg. Analogue Power	Regulated Power for Analogue	1.2V

GNDA		Power	Analogue Ground	0V Analogue Ground	0V
AVDD		Power	Ext. Analogue Power	Ext. Power for Analogue	1.5V
AVSS		Power	ESD Return	0V Ground specific to ESD return	0V
ADCAL		I	Analogue	ADC Calibration	
GNDD		Power	Digital Ground	0V Digital Ground	0V
DVDD		Power	Ext. Digital Power	Ext. Power for Digital	1.5V
VDDD		Power	Reg. Digital Power	Regulated Power for Digital	1.2V
GNDD		Power	Digital Ground	0V Digital Ground	0V
DVDD		Power	Ext. Digital Power	Ext. Power for Digital	1.5V
VDDD		Power	Reg. Digital Power	Regulated Power for Digital	1.2V
padID(0:3)	Static	I	CMOS Pull-Up	Chip Address (4 pads)	1.5V
DVSS		Power	ESD Return	0V Ground specific to ESD return	0V
LCB_IN_padN	160	I	SLVS	Encoded COM L0 BCR input (160Mb/s)	
LCB_IN_padP	160	I	SLVS	Encoded COM L0 BCR input (160Mb/s)	
GNDD		Power	Digital Ground	0V Digital Ground	0V
CLK_padN	160	I	SLVS	Readout rate clock input	
CLK_PadP	160	I	SLVS	Readout rate clock input	
DVSS		Power	ESD Return	0V Ground specific to ESD return	0V
DAT	160	O	SLVS	DATA signal	
DATB	160	O	SLVS	DATA signal	
Right side signals					
abcup_pad		I	CMOS Pull-Down	Reserved	0
VDDD		Power	Reg. Digital Power	Regulated Power for Digital	1.2V
TESTOUTPUTB	MHz	O	CMOS 8mA	Output for test output (bar)	
GNDD		Power	Digital Ground	0V Digital Ground	0V
unconnected input	MHz	I	CMOS Pull-Down		0
GNDD		Power	Digital Ground	0V Digital Ground	0V
TESTOUTPUT	MHz	O	CMOS 8mA	Output for test output	
GNDD		Power	Digital Ground	0V Digital Ground	0V
unconnected input	MHz	I	CMOS Pull-Down		0
GNDD		Power	Digital Ground	0V Digital Ground	0V
unconnected input	Static	O	CMOS Pull-Down		0
VDDD		Power	Reg. Digital Power	Regulated Power for Digital	1.2V
GNDD		Power	Digital Ground	0V Digital Ground	0V
padTESTCOM	Analogue	O	Analogue	Discriminator bias "spy" point	
TESTRES	Analogue	I	Analogue	Reference resistance	R
GNDA_local		Power	Analog Ground	0V Analogue Ground	0
AMUXOUT	Analogue	O	Analogue	Analogue "spy" output	

Table 7.1: ABCStarV1 Pad List

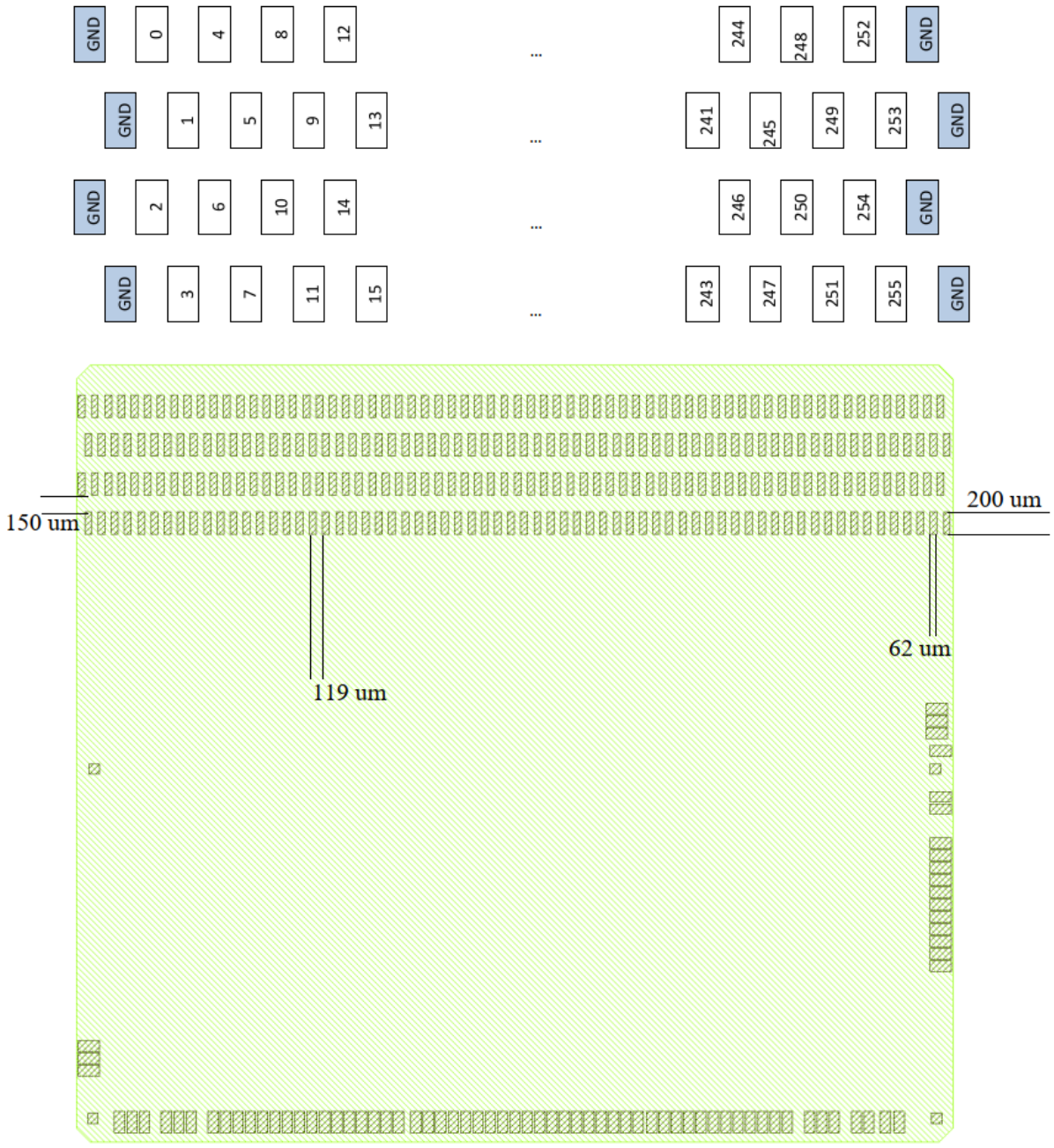

Figure 7.1: ABCStarV1 FE pads

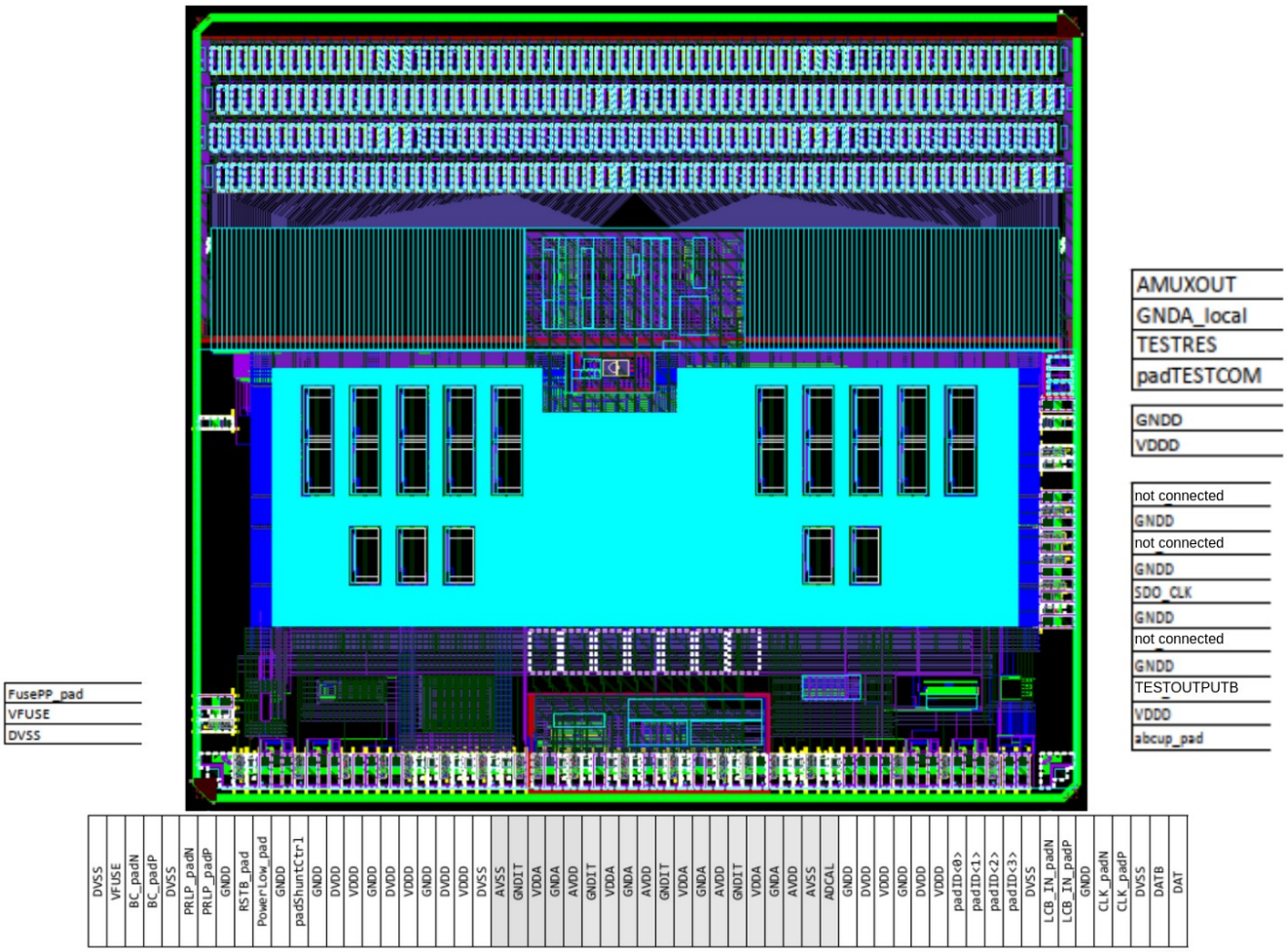

Figure 7.2: ABCStarV1 BE pads

8 Manufacturer

The ABCStarV1 will be fabricated in Global Foundry (Ex-IBM foundry) in the CMOS8RF_DM 130 nm technology. The wafers are standard 8 inches and will be thinned to $300 \pm 20\,\mu$m. No packaging is foreseen as the chip will be directly wirebonded to the hybrid.

9 Power

The internal power supply grid is divided into two power domains, analogue and digital. These power domains are powered by two independent on-chip linear voltage regulators. Pulling up the PowerLow_pad input to DVDD disables the reference line for the analog linear voltage regulator as well as reference line for the analog bias block and the SLVS I/O pads. The chip is in what is called "low power mode". The residual voltage at the analog VDD (VDDA) line is around 0.55V and with the minimum analog bias setting the chip still consumes about 8mA analog current. The digital voltage regulator is not affected by this signal. The power consumed by the digital part is effectively lowered by disabling digital I/O pads, i.e., disabling the bias of the I/O, and the clock distributed to the chip. In order to supply the chip with the external power supply while bypassing the linear regulators, the output voltage settings should be put to minimum value. This will ensure that the pass transistor of the regulator is not conducting. A shunt device controlled with the ShuntCtrl analogue signal is provided to equalize the currents of different ABCStar chips. Pulling down the padShuntCtrl signal to GND disables the shunt regulator. The shunt regulators must allow connecting their outputs in parallel on the hybrid even if the output voltages of the individual devices are not perfectly matched. It is required that only devices with an output voltages mismatch of within a range 100 mV can be connected in parallel.

9.1 Shunt Device

The shunt device consists of only one large shunt power device. The input ShuntCtrl has to be connected to a feedback control circuitry outside of ABCStar to control it. If no control is provided, it is good practice to hard connect ShuntCtrl to GND, so that the shunt device cannot draw any current from the power supply.

		Min	Nominal	Max
Minimum shunt current	Ishuntmin	1 uA	30 mA @ ShuntCtrl = .6V	150 mA @ ShuntCtrl = 1.5V
Internal shunt current limit	Ishuntlimit0	1 uA	250 mA @ ShuntCTRL = 2.2 V with Vdd = 0.1 V	
Disable inputs	ShuntCtrl		GND	
Response Time (0-90%)	ShuntCntrl		75 ns	

Table 9.1: Shunt regulator specifications

9.2 Voltage Regulators

9.2.1 Analogue Voltage Regulator

The analogue voltage regulator provides the voltage to the front-end circuitry.

9.2.2 Digital Voltage Regulator

This digital voltage regulator provides the voltage to all the digital circuitry in general.

9.2.3 Core Voltage Regulator

The DC power supply voltages requirements are defined below and apply to the core of the ABCStar chip. These will be delivered either from the internal on chip power management circuitry or from the

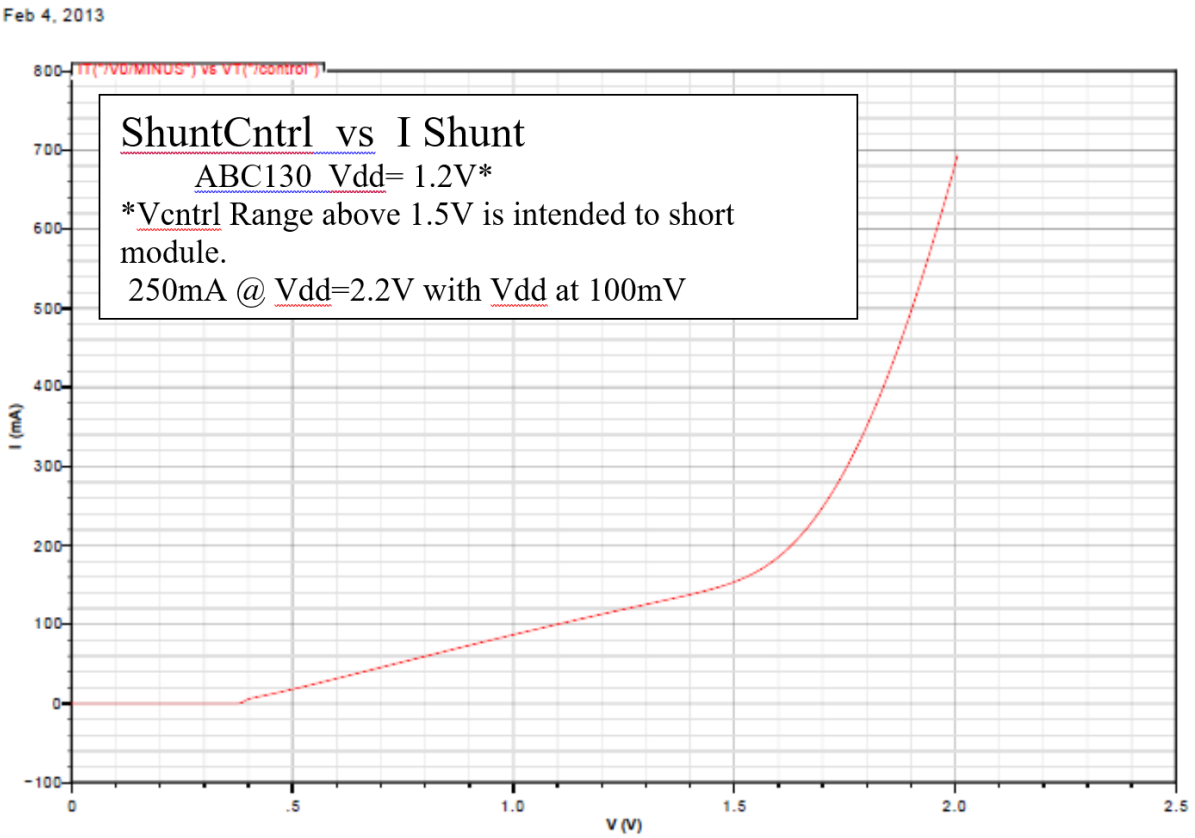

Figure 9.1: ABCStarV1 ShuntCntrl vs IShunt

		Min	Nominal	Max
Input Voltage	AVDD	1.25 V	1.50 V	1.60 V
Output voltage	VDDA	1.15 V	1.2 V	1.25 V
Output current	IDDA		70mA	

Table 9.2: Analogue voltage regulator specifications. 1.60 V is the limit imposed by the technology reliability parameters. The regulator circuit has been proven to operate at higher VDD up to 2V (for short time)

		Min	Nominal	Max
Input Voltage	DVDD	1.25 V	1.50 V	1.60 V
Output voltage	VDDD	1.00 V	1.20 V	1.25 V
Output current	IDDD		140 mA	
Output Impedance			0.3 ohm	
Rejection Ratio				
Rejection Ratio with 100nF external capacitor				

Table 9.3: Digital voltage regulator specification. 1.60 V is the limit imposed by the technology reliability parameters. The regulator circuit has been proven to operate at higher VDD up to 2V (for short time). 1.0V is the low range limit of the voltage regulator output. It does not mean that the chip is guaranteed to operate with this low voltage during its lifetime, especially because of the radiation effects.

external power sources via bond pads. The expected typical power consumption for nominal bias power supply voltages and bias currents: less than 1 mW/channel .

	Pad Name	Min	Nominal	Max	Absolute Max
Analogue Supply (1)	VDDA	1.15	1.2	1.25	1.6
Analogue Ground	GNDA		0		-0.3
Digital Supply (2)	VDDD	1.00	1.2	1.25	1.6
Digital Ground	GNDD		0		-0.3

Table 9.4: DC supply voltages. DC supplies are the ones applied to the analogue circuits, from either an output source or from the internal analogue voltage regulator. (1): DC supplies are the ones applied to the digital circuits, from either an output source or from the internal digital voltage regulator. (2): 1.0V is the low range limit of the voltage regulator output. It does not mean that the chip is guaranteed to operate with this low voltage during its lifetime, especially because of the radiation effects.

The current draw at each DC input is as follows (values excluding the regulator's current).

		Min	Nominal	Max
Analogue Supply	VDDA		70mA	
Analogue Ground	GNDA			
Digital Supply, Main regulator	VDDD		27 mA	
Digital Ground	GNDD			

Table 9.5: DC supply currents for the nominal voltage supplies (VDDA=1.2V, VDDD=1.2V) and nominal operating conditions; These are the nominal values after configuration. The values may change with configuration, and are increased by a factor 1 to 3 when the TID dose is between 1 and 10Mrad.

		Min	Nominal	Max
Analogue Supply	VDDA	43mA	70mA	100mA
Digital Supply	VDDD		27mA	

Table 9.6: Absolute Min/Max current draws at power supply inputs which may occur in non-standard operating conditions, e.g. all bias DACs set at zero or to full range, clock not supplied to the chips

10 Input/Output

10.1 SLVS input

Input Levels for SLVS Inputs (CLK, BC, LCB_IN, PRLP).

Parameter	Conditions	Minimum	Maximum
Input Voltage Range Vi		0	Vdd
InputVoltage Common mode Vicm		0.2V	1.0V
Effective Input Offset	MC result	0V	+/-10mV
Receiver input impedance		>1M Ω	

Table 10.1: Input Levels for SLVS Inputs (CLK, BC, LCB_IN, PRLP)

10.2 SLVS output

The differential driver is the same as in the HCCStarV0 ASIC. The driver is based on a full-bridge driver topology built with NMOS-PMOS switches which uses a termination resistor at the receiver side as a differential load. The bridge is supplied with two current sources (top and bottom). The current sources are programmable and their current is set by connecting/disconnecting the gates of the mirroring devices to the reference node. This architecture is rather weak w.r.t radiation as under radiation the Vth of the devices drifts depending on their gate voltage. However the effect should not be critical since the programmable space is only comprised of 3 bits and the programmed driving strength is not assumed to change during operation. The common-mode is set with a resistive divider, parallel to the switch bridge, and is of about half the power supply.

Parameter		Minimum	Maximum
Output Current	8 programmable steps	1mA	7mA
Output offset Voltage	Symmetric Drive		0
Output Differential Voltage	With 75 Ω Termination	75mV	520mV
Output impedance		k Ω	

Table 10.2: Output Levels for SLVS Outputs (DAT)

10.3 Input/Output ESD protections

The inputs and outputs signal pads use in general SOFICS protection with double SCR devices. The inputs have 50 Ohm (except for Front-End pads which have a 22 Ohms resistor) to improve the protection against CDM events. The outputs do not have a resistor. These structures offer the advantage of a very low input capacitance that is compatible with the multidrop techniques of differential signalling like clocks, LCB_IN and the LPPR. The exception is the padShuntCtrl that has dual gate non silicide NMOS protection device with a 50 Ohm resistor. The protection should stand a 2kV HBM (Human Body Model) event and a 100V Machine Model (MM). One of the characteristics of this ESD device is its low capacitance, below the values of the standard ESD protections of the foundry (200 fF vs 4 pF).

11 Detailed Description and Specification

11.1 Detector parameters

The design of the ABCStarV1 will be optimised for performance with barrel short strips. The post-radiation parameters of the different types of sensors, as understood presently, combined with the estimated parameters of the front end, are summarised in Table 11.1.

11.2 Front-end

11.2.1 Electrical Requirements

Note that the notation convention for currents used in the entire specification is "+" for current going into (sunk by) the chip and "-" for current going out of (sourced from) the chip.

11.2.2 Input Characteristics

Input Signal Polarity: The front-end circuit accepts negative signals from n-type strips

Crosstalk (via detector interstrip capacitance): The crosstalk should stay below 5% in the nominal biasing conditions with the maximum strip length (5.4cm)

Open Inputs: Any signal input can be open without affecting performance of other channels.

Input Protection: The front-end input is protected with a specially developed ESD structure (SOFICS BVBA, Belgium) using a SCR protection device. A simplified schematic is reproduced in figure 11.2.

	Endcap Ring 0 Φ= 1.61e15	Endcap Ring 1 Φ= 1.35e15	Endcap Ring 2 Φ= 1.19e15	Endcap Ring 3 Φ= 1.10e15	Endcap Ring 4 Φ= 0.97e15	Endcap Ring 5 Φ= 0.87e15	Barrel Short Strips Φ=	Barrel Long Strips Φ= 0.57e15 neq/cm^2
Coupling type to amplifier	AC						AC	
Readout strip implant	N						N	
Strip pitch	77.2 µm	71.3 µm	76.8 µm	73.6 µm	77.0 µm	77.7 µm	74.5 µm	
Strip Length	1.9 cm	2.4 cm	3.1 cm	2.9 cm	5.4 cm	5.0 cm	2.4 cm	4.8 cm
Coupling capacitance to amp	45.6 pF	76.5 pF	75.0 pF	69.8 pF	130.7 pF	120.3 pF	57.3 pF	114.5 pF
Sensor capacitance of strip to all neighbour strips	1.59 pF	2.15 pF	2.62 pF	2.52 pF	4.56 pF	4.17 pF	1.96 pF	3.91 pF
Sensor capacitance of strip to backplane	0.59 pF	0.75 pF	0.97 pF	0.90 pF	1.69 pF	1.55 pF	0.74 pF	1.48 pF
Possible added capacitance due to gluing hybrid to sensor	0.5 pF	0.5 pF	0.5 pF	0.5 pF	0.5 pF	0.5 pF	0.5 pF	0.5 pF
Total Load Capacitance ~ENC$_{serial}$ @bias 80/160uA	2.18-2.68 pF	2.90-3.40 pF	3.59-4.09 pF	3.42-3.92 pF	6.25-6.75 pF	5.72-6.22 pF	2.70-3.20 pF	5.39-5.89 pF
Metal strip resistance	57 Ω	72 Ω	94 Ω	87 Ω	163 Ω	150 Ω	72 Ω	143 Ω
Bias Resistor	1.5 MΩ	1.5 MΩ	1.5 MΩ	1.5 MΩ	1.5 MΩ	1.5 MΩ	1.5 MΩ	1.5 MΩ
Max leakage current per strip for shot noise and shot noise estimation	121-134 nA	118-131 nA	145-161 nA	120-133 nA	206-229 nA	171-190 nA	96-106 nA	100-113 nA
Collected charge (at 500 V), estimate from neutrons (conservative), [ke-]	8.6	9.4	9.9	10.3	10.8	11.3	10.4	13.1
Collected charge (at 500 V), estimate from charge/neutral mix, [ke-]	9.5	10.3	10.8	11.1	11.6	12.0	12.3	14.4
Maximum threshold assuming 50% charge division, 10% overdrive and Landau most probable/min) S/T >3.4	2800e-	3030e-	3180e-	3260e-	3410e-	3530e-	3620e-	4230e-
Maximum noise assuming 4 sigma distance to threshold	700e-	750e-	790e-	810e-	850e	880e-	900e	1050e-

Figure 11.1: Assumed detector electrical parameters

It consists of two SCR HBM protection devices connected through a 22 Ohm series resistor making the Ron resistance of the SCR negligible (CDM style protection). A single SCR protection device is qualified for 1kV HBM (Human Body Model) event and a 100V Machine Model (MM). The characteristics of this ESD device are a low trigger voltage (3V) and a low holding voltage (1.9V), well below the values of the standard ESD protections of the foundry (5V and 4V, respectively). The very low Ron (below 1 Ohm) should help to sustain charge deposition that occurs in case of detector breakdown. The equivalent capacitance loading to the front end input should be around 0.2pF (2x SCR).

11.2.3 Preamplifier-Shaper Characteristics

Gain at the discriminator input: 85 mV/fC for the nominal bias currents and the nominal process parameters

Effective gain extracted from the response curve: 80 mV/fC for the nominal bias currents and the nominal process parameters

Linearity:
better than 5% in the range 0 to -4 fC
better than 15% in the range 0 to -8 fC

Peaking time: 21 ns
Intrinsic peaking time of 21 ns of the circuit ensures a peaking time below 25 ns including the effect of charge collection time.

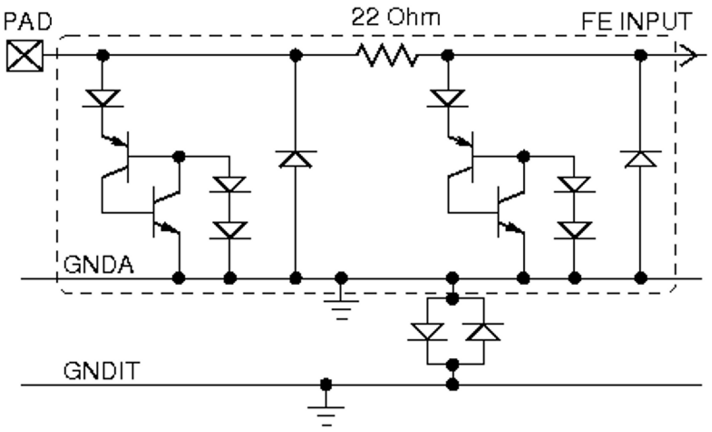

Figure 11.2: Frontend Input ESD protection

Noise: See Table 11.1 for maximum RMS noise allowable on fully populated modules after irradiation.

Gain Sensitivity to analogue supply voltage: for 1 fC signal: $< 5\%/100\text{mV}$

Power Supply Rejection Ratio: Check table Power Supply Rejection Ratio (not design targets but simulation results of the circuit)

Comparator Stage:
A threshold is applied as a differential voltage offset to the comparator stage. This threshold voltage is applied from an internal 8-bit DAC (bits BVT(0:7)).
Threshold setting range: 0V to -550mV, nominal setting at -80mV (-1fC) before irradiation and as low as -40mV (-0.5 fC) after full dose.
Test MUX output (AMUX decimal 9): TEST_THDAC MIN/MAX = 2mV/132mV
Threshold setting step without trimming: 2.3mV (8-bit resolution)
Threshold spread before trimming: < 15 mV RMS
The replicas of the DC threshold voltage (VTHTEST) and threshold voltage reference (VTHTESTREF) are available through AMUX.
The range of 5 bit trim DACs inside the channel is controllable with 5-bit DAC (bits BTRANGE(0:4)).
TrimDAC threshold setting range: MIN/MID/MAX: 50mV/150mV/230mV (controllable with 5 bit DAC)
TrimDAC resolution: MIN/MID/MAX: 5 bit (step 1.55mV/5mV/8mV)
TEST_TRDAC: MIN/MID/MAX (AMUX bit 0): 25mV / 65mV / 105mV

Strip length [cm]	2.4	4.8
10Hz-10kHz	57dB	57dB
10kHz-1MHz	17dB	16.5dB
1MHz-10MHz	6dB	6dB
10MHz-100MHz	3.5dB	3dB

Table 11.1: Power Supply Rejection Ratio

11.2.4 Timing Requirements

Time walk: 16 ns. This specification depends on the precision of the digital acquisition latch edge. Good alignment, 1 or 2 ns over a common clocked array of channels implies a longer time walk assignment to the rising edge of the shaped signal.

Time walk defined: For non-irradiated detectors; the maximum time variation in the crossing of the time stamp threshold over a signal range of -0.75 to -10 fC, with the comparator threshold set to -0.5 fC; For non-irradiated detectors time walk is in the range of 12.5ns For different cases of irradiated detectors please refer to Table 11.1.

Double Pulse Resolution: $\leq$ 75 ns for a -3.5 fC signal followed by a -3.5 fC signal at -0.5fC threshold

Max recovery time: Max recovery time for a -3.5 fC signal following -80 fC signal: 600ns

11.2.5 Calibration circuit

Calibration signal distributed with one calibration line can be applied to on-chip calibration capacitor (60fF) connected to front end input with CMOS switch controlled with one of the channel configuration bit. Address and the number of connected channels to the calibration line, as well as the amplitude of the calibration signal and its delay is set via the control logic. The voltage applied to the Calibration Capacitors by the chopper is determined by an internal 9-bit DAC. The calibration line is also brought through analog test mux to pad where the calibration voltage can be directly measured during the screening of the chip (analog test mux address 7). A tuneable delay of the calibration strobe with respect to the clock phase covering at least two clock periods is provided. The delay is built in chain of delay cells designed with current starved inverters and it is controlled with 6-bit register (bits STR_DEL<0:5>). The absolute delay magnitude is obtained by the calibration delay scans using known BC period with high input signals and low discriminator threshold. In order to compensate for the process variation a 2 bit register to set the range of the strobe delay is provided (bits STR_DEL_RANGE<0:1>). For nominal corner of the technology process the delays of the calibration strobe can be obtained are described in table 11.2.

STR_DEL_RANGE	2'b00	strobe disabled
STR_DEL_RANGE	2'b01	delay 0 to 50ns
STR_DEL_RANGE	2'b10	delay 0 to 60ns
STR_DEL_RANGE	2'b11	delay 0 to 80ns

Table 11.2: STR_DEL_RANGE delay range

Calibration Capacitors: 60 fF - 10% (3 sigma) over full production skew, 1% (3 sigma) within one chip.

Calibration signal, amplitude range: 0 – 170 mV (charge range: 0 – 10 fC)

amplitude step: 0.332 mV (charge step: 0.0195 fC)

Absolute accuracy of amplitude: to be calibrated during chip preselection.

Calibration DAC: is controlled through bits BCAL<0:8> of the control registers.

11.2.6 Biasing circuitry and output test multiplexer

The preamplifier input transistor and feedback bias currents are controlled by the internal 5-bit DAC converters referenced to the internal bandgap circuit. The predicted variation of the bandgap reference is of the order of +/- 40mV pk-pk over 592mV nominal value. In order to compensate for the variations of the bandgap reference voltage as well as for the variation of the resistors setting the bias currents, the internal bias reference generators can be calibrated with 5-bit DACs.

To adjust internal bias for voltages VCD and VB one should set bits BVREF(0:4). For nominal technology parameters BVREF = 4'b01101 should give TEST_VR = 80mV (nominal). To adjust internal bias for bias current generators (eg, the internal nodes IPRE, IBUF, IBDIFF, IBDIFFH) one should set bits BIREF(0:4). For nominal technology parameters, setting BIREF to 01111 should provide nominal bias of the input transistor around 140uA (TEST_IR =90mV). For this setting, the current consumption of the complete front end (256 channels, bias and calibration block, regulator) will be around 70mA. The useful range of the current biases, providing good operating points for all the devices independently of the process corner variation, are for BIREF settings between 00110 (TEST_IR=65mV) and BIREF=11001 (TEST_IR=116mV) equivalent to the bias of the input transistor in the range between 110 and 180uA (nominal process parameters). The current consumption of the front end for settings BIREF=00000 (state after power on reset) and BIREF=11111 are in the range of 43 and 100mA respectively (assuming nominal value of the BandGap reference). For the variation of the bias currents between 00110 and 11001

one should expect the variation of the gain in the order of 30%, ENC 15% (@ 7pF input capacitance) and the peaking time between 20 and 25ns (22ns for nominal settings).

To adjust internal bias for 8-bit threshold and calibration DACs one should set bits B8BREF<0:4>. For nominal technology parameters B8BREF=01101 should give TEST_R8B =80mV (nominal).

ICOM (comparator bias), register bits: BICOM<0:4>

Nominal value (MSB-LSB 10000): 9uA

MIN/MAX (00000/11111): 5uA/13uA

Test output: TESTCOM [MIN/NOM/MAX] = 20mV/35mV/52mV

11.2.7 Analog test multiplexer

For testing purposes the front end block is equipped with analog test multiplexer which is controlled through configuration registers. It connects the test points located in the bias block through switches to common line connected to the output pad. The ADC has a resolution of 1V/12bit and only features one gain stage. An additional gain stage between testpoints and the ADC input could have been implemented (as all measurements are around 100 mV and 600 mV) but it would have to be very high performant to achieve good accuracy, ie, it will take an increase of area and power consumption. The area of the ADC in the ABCStar was optimized for its optimal position in the floorplan. The analog test MUX is presented in the table 11.3. The access to the analog multiplexer is through the passive analog pad AMUXOUT or via internal monitoring ADC. The access to the test point of the DAC used for bias of the discriminator (supplied with digital power domain) is at the pad TESTCOM.

Decimal 0	n/a	output unconnected
Decimal 1	TEST_TRIM_DAC	range set by BTRANGE<0:4> register
Decimal 2	TEST_VR	nominal value =80mV : to be adjusted with BVREF<0:4>
Decimal 3	TEST_IR	nominal value =80mV : to be adjusted with BIREF<0:4>
Decimal 4	TEST_R8B	nominal value =80mV : to be adjusted with B8BREF<0:4>
Decimal 5	VCD	bias voltage (diff stage cascode): nominal value 550mV
Decimal 6	VB	bias voltage (diff stage input DC): nominal value 600mV
Decimal 7	VBG	bandgap voltage : nominal value 592mV
Decimal 8	CALLINE	calibration line
Decimal 9	TEST_THDAC	test point of the threshold DAC
Decimal 10	VTHTEST	replica of the threshold voltage; should be compared with VTHTESTREF
Decimal 11	VTHTESTREF	replica of the threshold voltage reference
Decimal 12	GNDA	local analog ground

Table 11.3: Analog test MUX

11.2.8 ADC for internal Bias, voltage and temperature monitoring

For monitoring purposes the ABCStar chip has an internal 12 bits Wilkinson ADC that connects through an analog multiplexer to the front-end bias block, to the bandgap references (via test multiplexer described above), raw and regulated voltages, temperature sensor, and the external calibration signal provided via the chip pad ADCAL. The block schematic of the ADC monitoring block is shown in Figure 11.3.

The ADC analog multiplexer connection is controlled through the 4 bits ADC_Ch[3:0]. When enabled, the ADC is free-running, at a sampling frequency of approx. 10 kHz (for max. range signals). The ADC operation can be enabled/disabled (clock switched off) and also reset. The default value is disabled. After enabling, the ADC should be reset. The bias current can be adjusted to compensate bandgap variations, through the 4 bits ADC_Bias[3:0]. The default operation value of the ADC_Bias bits is 4b'1100. The bias current reduces to 10% of nominal value when applying the code 4b'0000. The 12 bits outputs of the ADC are latched at the end of each conversion cycle, together with the 4 bits identifying the analog multiplexer selection, the 4 bits indicating the bias adjustment and the ADC enable status bit.

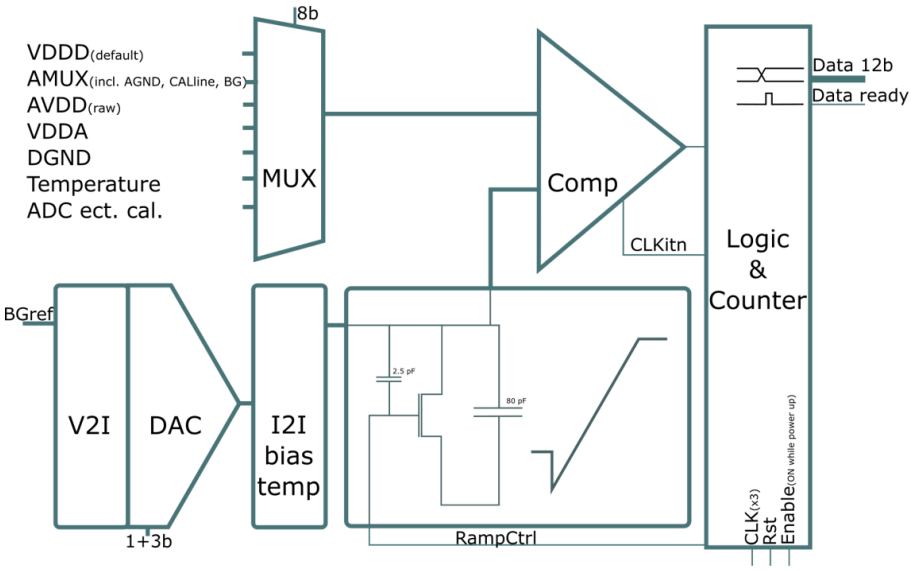

Figure 11.3: ADC monitoring block

The ADC's linear range is -25 mV to 900 mV and should be adjusted during calibration process.

For calibration the ADCAL pin can be used to connect an external reference signal to the ADC analog multiplexer (ADC_EXT_CALIBRATION in Table 11.4).

The ADCAL input ESD protection is using an ESD structure using double SCR protection device with 90 Ohm CDM resistor.

INL is better than 2 LSB for non-irradiated chips. INL is 3 LSB for irradiated chips.

Monitor	Exp. Range	MUX 4 bits setting
TESTVDDD (regulated digital)	0.5* VDDD	0000
AMUXOUT	0-800 mV	0001
TESTICOM		0010
TESTVDD (raw)	0.5*VDD	0011
TESTVDDA (regulated analog)	0.5*VDDA	0100
DGND (GND in digital)	0 mV	0101
TEMPERATURE	550-830 mV	0110
ADC_EXT_CALIBRATION	ADCAL input	1xxx

Table 11.4: Internal ADC analogue MUX

11.3 Channel Order and Channel Numbering

Channel identification in Physics data packets is done as follows:

- the row of strips with pads nearest to an ABCStar are given addresses 0 to 127
- the row of strips with pads furthest from an ABCStar are given addresses 128 to 255

The arrangement of the wire bonds from the detector to the input pads of the front-end channels is reported here for the barrel case. The mapping between detector strips, physical ABCStar pads, logical ABCStar channels and cluster addresses used in Physics packets is described in Table 11.5:

near strip	ABC Physical pad	ABC Logical channel	Cluster address in Physics packets (8b hex)		far strip	ABC Physical pad	ABC Logical channel	Cluster address in Physics packets (8b hex)
n0	0	0	0x00		f0	2	1	0x80
n1	1	2	0x01		f1	3	3	0x81
n2	4	4	0x02		f2	6	5	0x82
n3	5	6	0x03		f3	7	7	0x83
n4	8	8	0x04		f4	10	9	0x84
n5	9	10	0x05		f5	11	11	0x85
n6	12	12	0x06		f6	14	13	0x86
n7	13	14	0x07		f7	15	15	0x87
n8	16	16	0x08		f8	18	17	0x88
n9	17	18	0x09		f9	19	19	0x89
n10	20	20	0x0A		f10	22	21	0x8A
n11	21	22	0x0B		f11	23	23	0x8B
n12	24	24	0x0C		f12	26	25	0x8C
n13	25	26	0x0D		f13	27	27	0x8D
n14	28	28	0x0E		f14	30	29	0x8E
n15	29	30	0x0F		f15	31	31	0x8F
n16	32	32	0x10		f16	34	33	0x90
n17	33	34	0x11		f17	35	35	0x91
n18	36	36	0x12		f18	38	37	0x92
n19	37	38	0x13		f19	39	39	0x93
n20	40	40	0x14		f20	42	41	0x94
n21	41	42	0x15		f21	43	43	0x95
n22	44	44	0x16		f22	46	45	0x96
n23	45	46	0x17		f23	47	47	0x97
n24	48	48	0x18		f24	50	49	0x98
n25	49	50	0x19		f25	51	51	0x99
n26	52	52	0x1A		f26	54	53	0x9A
n27	53	54	0x1B		f27	55	55	0x9B
n28	56	56	0x1C		f28	58	57	0x9C
n29	57	58	0x1D		f29	59	59	0x9D
n30	60	60	0x1E		f30	62	61	0x9E
n31	61	62	0x1F		f31	63	63	0x9F
n32	64	64	0x20		f32	66	65	0xA0
n33	65	66	0x21		f33	67	67	0xA1
n34	68	68	0x22		f34	70	69	0xA2
n35	69	70	0x23		f35	71	71	0xA3
n36	72	72	0x24		f36	74	73	0xA4
n37	73	74	0x25		f37	75	75	0xA5
n38	76	76	0x26		f38	78	77	0xA6
n39	77	78	0x27		f39	79	79	0xA7
n40	80	80	0x28		f40	82	81	0xA8
n41	81	82	0x29		f41	83	83	0xA9
n42	84	84	0x2A		f42	86	85	0xAA
n43	85	86	0x2B		f43	87	87	0xAB
n44	88	88	0x2C		f44	90	89	0xAC
n45	89	90	0x2D		f45	91	91	0xAD
n46	92	92	0x2E		f46	94	93	0xAE
n47	93	94	0x2F		f47	95	95	0xAF
n48	96	96	0x30		f48	98	97	0xB0
n49	97	98	0x31		f49	99	99	0xB1

n50	100	100	0x32		f50	102	101	0xB2
n51	101	102	0x33		f51	103	103	0xB3
n52	104	104	0x34		f52	106	105	0xB4
n53	105	106	0x35		f53	107	107	0xB5
n54	108	108	0x36		f54	110	109	0xB6
n55	109	110	0x37		f55	111	111	0xB7
n56	112	112	0x38		f56	114	113	0xB8
n57	113	114	0x39		f57	115	115	0xB9
n58	116	116	0x3A		f58	118	117	0xBA
n59	117	118	0x3B		f59	119	119	0xBB
n60	120	120	0x3C		f60	122	121	0xBC
n61	121	122	0x3D		f61	123	123	0xBD
n62	124	124	0x3E		f62	126	125	0xBE
n63	125	126	0x3F		f63	127	127	0xBF
n64	128	128	0x40		f64	130	129	0xC0
n65	129	130	0x41		f65	131	131	0xC1
n66	132	132	0x42		f66	134	133	0xC2
n67	133	134	0x43		f67	135	135	0xC3
n68	136	136	0x44		f68	138	137	0xC4
n69	137	138	0x45		f69	139	139	0xC5
n70	140	140	0x46		f70	142	141	0xC6
n71	141	142	0x47		f71	143	143	0xC7
n72	144	144	0x48		f72	146	145	0xC8
n73	145	146	0x49		f73	147	147	0xC9
n74	148	148	0x4A		f74	150	149	0xCA
n75	149	150	0x4B		f75	151	151	0xCB
n76	152	152	0x4C		f76	154	153	0xCC
n77	153	154	0x4D		f77	155	155	0xCD
n78	156	156	0x4E		f78	158	157	0xCE
n79	157	158	0x4F		f79	159	159	0xCF
n80	160	160	0x50		f80	162	161	0xD0
n81	161	162	0x51		f81	163	163	0xD1
n82	164	164	0x52		f82	166	165	0xD2
n83	165	166	0x53		f83	167	167	0xD3
n84	168	168	0x54		f84	170	169	0xD4
n85	169	170	0x55		f85	171	171	0xD5
n86	172	172	0x56		f86	174	173	0xD6
n87	173	174	0x57		f87	175	175	0xD7
n88	176	176	0x58		f88	178	177	0xD8
n89	177	178	0x59		f89	179	179	0xD9
n90	180	180	0x5A		f90	182	181	0xDA
n91	181	182	0x5B		f91	183	183	0xDB
n92	184	184	0x5C		f92	186	185	0xDC
n93	185	186	0x5D		f93	187	187	0xDD
n94	188	188	0x5E		f94	190	189	0xDE
n95	189	190	0x5F		f95	191	191	0xDF
n96	192	192	0x60		f96	194	193	0xE0
n97	193	194	0x61		f97	195	195	0xE1
n98	196	196	0x62		f98	198	197	0xE2
n99	197	198	0x63		f99	199	199	0xE3
n100	200	200	0x64		f100	202	201	0xE4
n101	201	202	0x65		f101	203	203	0xE5
n102	204	204	0x66		f102	206	205	0xE6
n103	205	206	0x67		f103	207	207	0xE7
n104	208	208	0x68		f104	210	209	0xE8

n105	209	210	0x69		f105	211	211	0xE9
n106	212	212	0x6A		f106	214	213	0xEA
n107	213	214	0x6B		f107	215	215	0xEB
n108	216	216	0x6C		f108	218	217	0xEC
n109	217	218	0x6D		f109	219	219	0xED
n110	220	220	0x6E		f110	222	221	0xEE
n111	221	222	0x6F		f111	223	223	0xEF
n112	224	224	0x70		f112	226	225	0xF0
n113	225	226	0x71		f113	227	227	0xF1
n114	228	228	0x72		f114	230	229	0xF2
n115	229	230	0x73		f115	231	231	0xF3
n116	232	232	0x74		f116	234	233	0xF4
n117	233	234	0x75		f117	235	235	0xF5
n118	236	236	0x76		f118	238	237	0xF6
n119	237	238	0x77		f119	239	239	0xF7
n120	240	240	0x78		f120	242	241	0xF8
n121	241	242	0x79		f121	243	243	0xF9
n122	244	244	0x7A		f122	246	245	0xFA
n123	245	246	0x7B		f123	247	247	0xFB
n124	248	248	0x7C		f124	250	249	0xFC
n125	249	250	0x7D		f125	251	251	0xFD
n126	252	252	0x7E		f126	254	253	0xFE
n127	253	254	0x7F		f127	255	255	0xFF

Table 11.5: Relationship between physical FE pads, logical channels and cluster addresses

11.4 Clock and Control Signals

The table 11.6 defines the ABCStar clock and data signals.

Name	Type	Description
RCLK	SLVS	160MHz Clock input primarily intended for Data Readout
BC	SLVS	Beam Crossing Clock at 40MHz
LCB_IN	SLVS	160Mb/s, L0 Synchronous Trigger, L0tag, CMD and BCR bits
PRLP	SLVS	80Mb/s, PR with BC falling edge, LP with BC rising edge

Table 11.6: Clock and Control Signals

RCLK: The readout clock is used to clock data out of the chip. It runs at 160 MHz. This clock will be precisely phase shifted, under control of the HCCStar ASIC, with respect to BC to provide optimal operation.

BC: This is the primary clock delivered through the stave that samples the analogue channels outputs. The BC clock will be delayed by an arbitrary amount with respect to the incoming stave clock to accommodate a hybrid wide phase shift to align sensor signals with the BC.

LCB: The L0A/CMD/BCR (LCB) protocol is used to send L0 triggers, commands and bunch counter resets with respect to the RCLK 160MHz clock. A single unit is a frame consisting of two 8-bit symbols covering 4 BC. Symbols may either be 6 bits of payload, encoded using 6b8b or an 8-bit control symbol (K0, K1, K2 or K3). The LCB protocol is described further in section 11.5.

PRLP: This 80Mb/s signal is comprised of two time multiplexed 40Mb/s components

PR: The Priority Request (PR) signal is sampled on the falling edge of the BC clock and has two fields and a length of 10 bits : 3 bits act as start bit pattern (101), followed by 7 bits containing the L0tag identifier of the event to retrieve in the EvtBuffer. The idle state between consecutive PR commands is zero with at least one zero separating 2 consecutive PRs.

LP: The Low Priority Request (LP) signal is sampled on the rising edge of the BC clock and has two fields and a length of 10 bits : 3 bits act as start bit pattern (110), followed by 7 bits containing the L0tag identifier of the event to retrieve in the EvtBuffer. The idle state between consecutive LP commands is zero with at least one zero separating 2 consecutive LPs.

11.5 LCB Signaling and Protocol

The L0A/CMD/BCR (also known as LCB) signal transfers triggers (L0A), fast commands, register reads and writes (CMD) and bunch counter resets (BCR) to the HCCStar and then onto the ABCStar. The signal is 6b8b encoded and sent at 160Mbps over an LVDS bus that is shared by between two and ten HCCStar ASICs that in turn feed it to between seven to eleven ABCStar ASICs, depending on hybrid type. The serial stream is synchronous with the BC, although not necessarily in-phase. The ABCStar must "lock" onto the LCB stream at initialisation. The basic unit of data transmission is a pair of 8-bit symbols called a frame, providing 12 bits of payload per frame. Frames have five distinct frame-types – Idle, L0A, Fast Command (incl. resets), K2 (for start and end of slow command sequences) and slow command payload frames.

11.5.1 LCB Locking Mechanism

The 160Mbps LCB signal needs to be sampled (and pipelined) by a 160MHz clock on the ABCStar (RCLK). This clock is provided by the HCCStar. The ABCStar will sample the 4 pipelined LCB bits on the BC rising edge, with the HCC responsible for setting the correct phase between the BC clock, RCLK, LCB data and the PR/LP data. The ABCStar will "lock" onto the LCB - this is achieved by counting idle-frames (count up) and bad 6b8b symbols (count down). When 16 correct symbols are seen, the link is considered "locked", and decoding can proceed. When locked, the counting will continue, but the output of the 8b6b decoder is used to increment/decrement the counter instead. 15 consecutive bad 6b8b symbols will unlock the link. In normal operation the High Priority Register (HPR) packet will be sent at regular intervals. It includes information to assist off-detector firmware or software to modify settings to achieve lock. This is described further in section 11.14.6.

11.5.2 L0A/BCR

Since the LCB signal is transmitted at a data rate of 160 Mbps, a single frame takes 100 ns, or 4 BC, to transmit. Thus, a frame containing L0A data must cover 4 BC worth of L0A activity information. With an L0A, a 7-bit identifier, called the L0tag, is sent. This identifier is used to request event data from the ABCStar. In addition, the BCR signal may come during a 4 BC space that has L0As. The payload for an L0 frame is shown in Table 11.7. The msb of the L0A mask refers to the earliest BC, while the lsb refers to latest. A '1' in the L0A mask indicates that there is an L0A in the corresponding BC. A '1' in the BCR field indicates that there is to be a BCR in the latest BC covered by the L0A mask.

It is important to note that this implies that frames must have a fixed alignment with respect to the LHC orbit signal in order to guarantee that the BCR is executed at the front-end at the appropriate time.

L0A frames are only sent when at least one of the covered BC has an L0A or a BCR needs to be sent. Therefore, at least one of the first five bits will be '1'.

Note: when no triggers or BCRs are present, in other words, if the first 5 bits are all zero, this frame type is used to transfer slow command (CMD) payload data (for more details, see section 11.5.4).

	MSB		LSB
Field Name	BCR	L0A mask	L0tag
# of bits	1	4	7

Table 11.7: LCB L0 Frame

11.5.3 Fast Commands and Resets

Fast commands and resets are sent with a frame that contains the 6b8b control symbol K3 plus a symbol whose payload is composed of a 2-bit BC selector, indicating in which BC the command or reset is to be generated, and a 4-bit action indicating which command or reset to generate. A value of 0 for the BC selector refers to the earliest BC, while a value of 3 refers to the latest. The payload for the second symbol is shown in 11.8. The list of fast commands is show in Table 11.9. Note that fast commands are broadcast commands and are interpreted on all ASICs that share the LCB control line.

	MSB	LSB
Field Name	BC Select	Command
# of bits	2	4

Table 11.8: LCB K3 Frame Payload

Index	Command
0	No fast command
1	Reserved for future use
2	LogReset
3	RegReset
4	SEUReset
5	Cal Pulse
6	Digital Pulse
7	Hit Count Reset
8	Hit Count Start
9	Hit Count Stop
10	Slow Command Reset

Table 11.9: LCB Fast Commands

11.5.4 Register Reads and Writes

Register reads and writes are composed of a sequence of frames. These frames do not need to be consecutive, but must be in order. Frames interleaved in a register command sequence may be of any type. A register command sequence starts and ends with a "K2 frame" - composed of the K2 control symbol followed by a symbol containing an ABC/HCC select bit, a Start/End bit, and the HCC ID for the HCCStar on the target hybrid. If the ABC/HCC bit is '1' the command is an ABCStar command (otherwise it is an HCCStar command). If the Start/End bit is '1', it indicates the start of a command sequence ("K2 Start"), while '0' indicates it is the end of a command sequence ("K2 End"). An HCC ID of '1111' is interpreted to be a broadcast address and all ABCStar ASICs will respond. A special HCC ID of '1110' is used to indicate that the command sequence should be ignored. The HCC ID is used here because the LCB stream is common to HCCStar and ABCStar and the data format is maintained. When an HCCStar detects a K2 Start for a different HCCStar, it changes the K2 frame to have the special "ignore" HCC ID. The payload for the second symbol in this K2 frame is shown in Table 11.10. The K2 frame is followed by two header frames. The 5 MSBs of the header frames' payload are '00000' to distinguish these frames from L0 frames. The remainder of the payload is a Read/Write bit, the ABC ID of the target ABCStar ASIC and the address of the target register. If the Read/Write bit is '1', the command is a read command otherwise it is a write command. The mapping of these fields to the frame payloads is shown in Table 11.11. For register read commands, the header frames are followed by a K2 End frame (with the Start/End bit set to 0) indicating the end of the sequence. The K2 End resets the CMD decoder. The HCC ID field is ignored. For register write commands, the two header frames are followed by 5 frames containing the value to write into the register, as shown in Table 11.12. As with the register reads, the sequence ends with a K2 End frame. Register write commands can be issued without any intervening space between commands. Register access command sequences may be terminated at any time with a K2 End frame. While not encouraged, a K2 Start frame will terminate any pending

commands and start a new one. A new command sequence may immediately follow the K2 End frame. To guard against spurious register writes, the number of words in a command sequence is counted, and no action will be taken if the K2 End frame occurs at the wrong stage in the process.

	MSB		LSB
Field	ABC/HCC	Start/End	HCC ID
# of bits	1	1	4

Table 11.10: LCB K2 Frame Payload

Frame		MSB			LSB
1	Field	Marker	R/W	ABC ID	Reg Addr msb
	Value	00000			
	# of bits	5	1	4	2
2	Field	Marker		Reg Addr LSB	SPARE
	Value	00000			
	# of bits	5		6	1

Table 11.11: LCB Register Command Header Frames

Frame		MSB		LSB
1	Field	Marker	SPARE	Register contents [31:28]
	Value	00000		
	# of bits	5	3	4
2	Field	Marker		Register contents [27:21]
	Value	00000		
	# of bits	5		7
3	Field	Marker		Register contents [20:14]
	Value	00000		
	# of bits	5		7
4	Field	Marker		Register contents [13:7]
	Value	00000		
	# of bits	5		7
5	Field	Marker		Register contents [6:0]
	Value	00000		
	# of bits	5		7

Table 11.12: LCB Register Data Frames

11.5.5 Idle

The IDLE frame, composed of the control symbol pair K0, K1, will be sent if there is nothing else to send. This frame is used to establish initial synchronization on the link and provide for ongoing validation of synchronization.

11.5.6 Error Monitoring

The LCB system will provide information that off-detector firmware or software (or human operators) can used to diagnose link problems. In particular, information is needed about an un-locked LCB, such that the situation can be remedied. This will be achieved via the HPR mechanism, where information is automatically sent by the HCCStar (or ABCStar) when not locked. The following flags are available, and can be used by the HPR system, for example.

- Lock (LCB_Locked)
- LCB decoder Error (LCB_Decode_Err)
- LCB decoder error count too high (transgression of a threshold – LCB_ErrCnt_Ovfl)
- Error detected during a slow command sequence (LCB_SCmd_Err)
- LCB decoder errors (LCB_ErrCount)
- SEU detection

11.5.7 SEU Mitigation

State-machine state registers are Hamming coded. Logic influencing the locked status of the link will be protected using triple modular redundancy techniques. Flags and counts of errors will be provided.

11.6 Trigger Signals

Latency and other parameters associated with three trigger options being considered.

Parameter	
L0 rate	1 MHz
Prescription for worst case multiple L0s in consecutive BCs.	TBD
Prescription for worst case multiple PRs (ROIs) to the same region in consecutive BCs.	TBD
Max latency of L0 (at input to LTI and assumptions about arrival at ABCStar).	Alternate below
Max latency of L0 at output of FELIX (not clear what internal FELIX processing time is included)	10 us
Max latency to deliver data to L1Track in response to L0+PR. “First bit of requested data to leave HCC after a PR”	4 us
Assuming PRs are asynchronous, max delay of PR after L0.	3 us
Max latency of LP (at input to LTI and assumptions about arrival at ABCStar).	Alternate below
Max latency of LP at output of FELIX (not clear what internal FELIX processing time is included)	60 us
Max latency to deliver data to FELIX (or some other point) in response to LP.	No Limit

Table 11.13: Original Trigger Scheme: 1 MHz L0s, 10% PRs, 400 kHz LPs

Parameter	
L0 rate	1 MHz
Prescription for worst case multiple L0s in consecutive BCs.	TBD
Prescription for worst case multiple PRs (ROIs) to the same region in consecutive BCs.	NA
Max latency of L0 (at input to LTI and assumptions about arrival at ABCStar).	Alternate below
Max latency of L0 at output of FELIX (not clear what internal FELIX processing time is included)	10 us
Max latency to deliver data to L1Track in response to L0+PR. “Last hit leaving HCC after a PR” (not clear how to define this)	NA

Assuming PRs are asynchronous, max delay of PR after L0.	NA
Max latency of LP (at input to LTI and assumptions about arrival at ABCStar).	NA
Max latency of LP at output of FELIX (not clear what internal FELIX processing time is included)	NA
Max latency to deliver data to FELIX (or some other point) in response to LP.	NA

Table 11.14: Single Trigger Scheme: 1 MHz L0s – everyone reads everything out at L0

Parameter	
L0 rate	4 MHz
Prescription for worst case multiple L0s in consecutive BCs.	TBD
Prescription for worst case multiple PRs (ROIs) to the same region in consecutive BCs.	TBD
Max latency of L0 (at input to LTI and assumptions about arrival at ABCStar).	Alternate below
Max latency of L0 at output of FELIX (not clear what internal FELIX processing time is included)	4.5 us
Max latency to deliver data to L1Track in response to L0+PR. “First bit of requested data to leave HCC after a PR”	4 us
Assuming PRs are asynchronous, max delay of PR after L0.	1.8 us
Max latency of LP (at input to LTI and assumptions about arrival at ABCStar).	Alternate below
Max latency of LP at output of FELIX (not clear what internal FELIX processing time is included)	22.83 us (22 us proposed)
Max latency to deliver data to FELIX (or some other point) in response to LP.	No Limit

Table 11.15: Low Latency L0 Scheme: 2-4 MHz L0s, $< 10\%$ PRs, 600-800 LPs (with constraint that 10% PRs + LPs $<$ 1 MHz readout of everything)

11.7 Input Register and Test/Mask Register

The functions of the input register and test/mask register will be implemented in a single functional block.

11.7.1 Input Register

This register latches the incoming data with the rising edge of BC, delivering a clocked pulse to the subsequent circuits.

11.7.2 Channel Mask Register

This register serves a dual purpose. Firstly, the Channel Mask register enables any bad or noisy channels to be turned off thus preventing them from increasing the data rate due to false hits. Secondly, it can be used during chip testing to apply a set of test patterns to the pipeline. In the Mask mode, a channel is masked with ‘1’. In Test mode, there are two modes of operation, static and pulsed. In the Static Test Mode, the pipeline input gets continuously the Mask bit value. In the Test Pulse mode, there are 3 options controlled by a bit in one of the configuration registers:

- Option 1: the pipeline inputs get the Mask bit value for the duration of one clock period, otherwise it is always zero (no hit). The one clock period pulse is generated by the “Digital Test Pulse” Command applied through the LCB fast command protocol.
- Option 2: the pipeline inputs get a bit pattern along 4 consecutive BC. Two sets of 4 bit patterns are defined in configuration registers (bits 19 to 26 of the register at address $20). One set is applied to the channels with the Mask bit set and the other set is applied to the channels with the

Mask bit unset. The patterns are triggered by the “Digital Test Pulse” Command applied through the LCB fast command protocol.

- Option 3: A rotary fixed pattern with the BCIDcounter is used. Refer to table 11.17.

It is possible to enable (1) or disable (0) the test pulse signal in any mode. For all test modes, the front-end channels outputs are disabled (set to zero).

TM(1:0) bits	Mode of Operation
00	Normal Data Taking (Contents of register used to ”Mask Inputs”)
01	Static Test Mode (Contents of mask register are used to supply test values to pipeline)
10	Test Pulse Mode (2 options, see the description in the paragraph)
11	BCID fixed rotary pattern

Table 11.16: Test Mode: Masking Register Modes of Operation

BCID (decimal)	BCID[2:0] + xor(BCID)’hexa	C1’hexa	C2’hexa	C3’hexa	C4’hexa	lastbit_c1	lastbit_c2	lastbit_c3	lastbit_c4
0	0	7f0	3f8	7ff	7ff	0	1	0	0
1	3	7f0	3f8	7ff	7ff	0	1	0	0
2	5	3f8	7ff	7ff	7ff	1	0	0	0
3	6	400	7ff	7ff	7ff	1	0	0	0
4	9	400	008	7ff	7ff	0	1	0	0
5	a	400	008	7ff	7ff	0	1	0	0
6	c	00c	7ff	7ff	7ff	1	0	0	0
7	f	010	7ff	7ff	7ff	1	0	0	0
8	1	010	7ff	7ff	7ff	1	0	0	0
9	2	418	7ff	7ff	7ff	1	0	0	0
10	4	418	020	7ff	7ff	0	1	0	0
11	7	418	020	7ff	7ff	0	1	0	0
12	8	020	7ff	7ff	7ff	1	0	0	0
13	b	428	7ff	7ff	7ff	1	0	0	0
14	d	428	7ff	7ff	7ff	1	0	0	0
15	e	42c	7ff	7ff	7ff	1	0	0	0
16	1	430	038	7ff	7ff	0	1	0	0
17	2	430	038	7ff	7ff	0	1	0	0
18	4	03c	7ff	7ff	7ff	1	0	0	0
19	7	040	7ff	7ff	7ff	1	0	0	0
20	8	040	7ff	7ff	7ff	1	0	0	0
21	b	448	7ff	7ff	7ff	1	0	0	0
22	d	448	7ff	7ff	7ff	1	0	0	0
23	e	44c	7ff	7ff	7ff	1	0	0	0
24	0	450	058	7ff	7ff	0	1	0	0
25	3	450	058	7ff	7ff	0	1	0	0
26	5	058	7ff	7ff	7ff	1	0	0	0
27	6	460	7ff	7ff	7ff	1	0	0	0
28	9	460	068	7ff	7ff	0	1	0	0
29	a	460	068	7ff	7ff	0	1	0	0
30	c	06c	7ff	7ff	7ff	1	0	0	0
31	f	070	7ff	7ff	7ff	1	0	0	0
32	1	070	7ff	7ff	7ff	1	0	0	0
33	2	478	7ff	7ff	7ff	1	0	0	0
34	4	478	080	7ff	7ff	0	1	0	0
35	7	478	080	7ff	7ff	0	1	0	0
36	8	080	7ff	7ff	7ff	1	0	0	0
37	b	488	7ff	7ff	7ff	1	0	0	0
38	d	488	7ff	7ff	7ff	1	0	0	0
39	e	48c	7ff	7ff	7ff	1	0	0	0
40	0	490	098	7ff	7ff	0	1	0	0
41	3	490	098	7ff	7ff	0	1	0	0
42	5	098	7ff	7ff	7ff	1	0	0	0
43	6	4a0	7ff	7ff	7ff	1	0	0	0
44	9	4a0	0a8	7ff	7ff	0	1	0	0
45	a	4a0	0a8	7ff	7ff	0	1	0	0
46	c	0ac	7ff	7ff	7ff	1	0	0	0
47	f	0b0	7ff	7ff	7ff	1	0	0	0
48	0	0b0	7ff	7ff	7ff	1	0	0	0
49	3	4b8	7ff	7ff	7ff	1	0	0	0
50	5	4b8	7ff	7ff	7ff	1	0	0	0
51	6	4bc	7ff	7ff	7ff	1	0	0	0
52	9	4c0	0c8	7ff	7ff	0	1	0	0
53	a	4c0	0c8	7ff	7ff	0	1	0	0
54	c	0cc	7ff	7ff	7ff	1	0	0	0
55	f	0d0	7ff	7ff	7ff	1	0	0	0
56	1	0d0	7ff	7ff	7ff	1	0	0	0
57	2	4d8	7ff	7ff	7ff	1	0	0	0
58	4	4d8	0e0	7ff	7ff	0	1	0	0
59	7	4d8	0e0	7ff	7ff	0	1	0	0
60	8	0e0	7ff	7ff	7ff	1	0	0	0
61	b	4e8	7ff	7ff	7ff	1	0	0	0
62	d	4e8	7ff	7ff	7ff	1	0	0	0
63	e	4ec	7ff	7ff	7ff	1	0	0	0

64	1	4f0	0f8	7ff	7ff	0	1	0	0
65	2	4f0	0f8	7ff	7ff	0	1	0	0
66	4	0fc	7ff	7ff	7ff	1	0	0	0
67	7	100	7ff	7ff	7ff	1	0	0	0
68	8	100	7ff	7ff	7ff	1	0	0	0
69	b	508	7ff	7ff	7ff	1	0	0	0
70	d	508	7ff	7ff	7ff	1	0	0	0
71	e	50c	7ff	7ff	7ff	1	0	0	0
72	0	510	118	7ff	7ff	0	1	0	0
73	3	510	118	7ff	7ff	0	1	0	0
74	5	118	7ff	7ff	7ff	1	0	0	0
75	6	520	7ff	7ff	7ff	1	0	0	0
76	9	520	128	7ff	7ff	0	1	0	0
77	a	520	128	7ff	7ff	0	1	0	0
78	c	12c	7ff	7ff	7ff	1	0	0	0
79	f	130	7ff	7ff	7ff	1	0	0	0
80	0	130	7ff	7ff	7ff	1	0	0	0
81	3	538	7ff	7ff	7ff	1	0	0	0
82	5	538	7ff	7ff	7ff	1	0	0	0
83	6	53c	7ff	7ff	7ff	1	0	0	0
84	9	540	148	7ff	7ff	0	1	0	0
85	a	540	148	7ff	7ff	0	1	0	0
86	c	14c	7ff	7ff	7ff	1	0	0	0
87	f	150	7ff	7ff	7ff	1	0	0	0
88	1	150	7ff	7ff	7ff	1	0	0	0
89	2	558	7ff	7ff	7ff	1	0	0	0
90	4	558	160	7ff	7ff	0	1	0	0
91	7	558	160	7ff	7ff	0	1	0	0
92	8	160	7ff	7ff	7ff	1	0	0	0
93	b	568	7ff	7ff	7ff	1	0	0	0
94	d	568	7ff	7ff	7ff	1	0	0	0
95	e	56c	7ff	7ff	7ff	1	0	0	0
96	0	570	178	7ff	7ff	0	1	0	0
97	3	570	178	7ff	7ff	0	1	0	0
98	5	178	7ff	7ff	7ff	1	0	0	0
99	6	580	7ff	7ff	7ff	1	0	0	0
100	9	580	188	7ff	7ff	0	1	0	0
101	a	580	188	7ff	7ff	0	1	0	0
102	c	18c	7ff	7ff	7ff	1	0	0	0
103	f	190	7ff	7ff	7ff	1	0	0	0
104	1	190	7ff	7ff	7ff	1	0	0	0
105	2	598	7ff	7ff	7ff	1	0	0	0
106	4	598	1a0	7ff	7ff	0	1	0	0
107	7	598	1a0	7ff	7ff	0	1	0	0
108	8	1a0	7ff	7ff	7ff	1	0	0	0
109	b	5a8	7ff	7ff	7ff	1	0	0	0
110	d	5a8	7ff	7ff	7ff	1	0	0	0
111	e	5ac	7ff	7ff	7ff	1	0	0	0
112	1	5b0	1b8	7ff	7ff	0	1	0	0
113	2	5b0	1b8	7ff	7ff	0	1	0	0
114	4	1bc	7ff	7ff	7ff	1	0	0	0
115	7	1c0	7ff	7ff	7ff	1	0	0	0
116	8	1c0	7ff	7ff	7ff	1	0	0	0
117	b	5c8	7ff	7ff	7ff	1	0	0	0
118	d	5c8	7ff	7ff	7ff	1	0	0	0
119	e	5cc	7ff	7ff	7ff	1	0	0	0
120	0	5d0	1d8	7ff	7ff	0	1	0	0
121	3	5d0	1d8	7ff	7ff	0	1	0	0
122	5	1d8	7ff	7ff	7ff	1	0	0	0
123	6	5e0	7ff	7ff	7ff	1	0	0	0
124	9	5e0	1e8	7ff	7ff	0	1	0	0
125	a	5e0	1e8	7ff	7ff	0	1	0	0
126	c	1ec	7ff	7ff	7ff	1	0	0	0
127	f	1f0	7ff	7ff	7ff	1	0	0	0
128	1	1f0	7ff	7ff	7ff	1	0	0	0
129	2	5f8	7ff	7ff	7ff	1	0	0	0
130	4	5f8	200	7ff	7ff	0	1	0	0
131	7	5f8	200	7ff	7ff	0	1	0	0
132	8	200	7ff	7ff	7ff	1	0	0	0
133	b	608	7ff	7ff	7ff	1	0	0	0
134	d	608	7ff	7ff	7ff	1	0	0	0
135	e	60c	7ff	7ff	7ff	1	0	0	0
136	0	610	218	7ff	7ff	0	1	0	0
137	3	610	218	7ff	7ff	0	1	0	0
138	5	218	7ff	7ff	7ff	1	0	0	0
139	6	620	7ff	7ff	7ff	1	0	0	0
140	9	620	228	7ff	7ff	0	1	0	0
141	a	620	228	7ff	7ff	0	1	0	0
142	c	22c	7ff	7ff	7ff	1	0	0	0
143	f	230	7ff	7ff	7ff	1	0	0	0
144	0	230	7ff	7ff	7ff	1	0	0	0
145	3	638	7ff	7ff	7ff	1	0	0	0
146	5	638	7ff	7ff	7ff	1	0	0	0
147	6	63c	7ff	7ff	7ff	1	0	0	0
148	9	640	248	7ff	7ff	0	1	0	0
149	a	640	248	7ff	7ff	0	1	0	0
150	c	24c	7ff	7ff	7ff	1	0	0	0
151	f	250	7ff	7ff	7ff	1	0	0	0
152	1	250	7ff	7ff	7ff	1	0	0	0
153	2	658	7ff	7ff	7ff	1	0	0	0
154	4	658	260	7ff	7ff	0	1	0	0
155	7	658	260	7ff	7ff	0	1	0	0
156	8	260	7ff	7ff	7ff	1	0	0	0

157	b	668	7ff	7ff	7ff	1	0	0	0
158	d	668	7ff	7ff	7ff	1	0	0	0
159	e	66c	7ff	7ff	7ff	1	0	0	0
160	0	670	278	7ff	7ff	0	1	0	0
161	3	670	278	7ff	7ff	0	1	0	0
162	5	278	7ff	7ff	7ff	1	0	0	0
163	6	680	7ff	7ff	7ff	1	0	0	0
164	9	680	288	7ff	7ff	0	1	0	0
165	a	680	288	7ff	7ff	0	1	0	0
166	c	28c	7ff	7ff	7ff	1	0	0	0
167	f	290	7ff	7ff	7ff	1	0	0	0
168	1	290	7ff	7ff	7ff	1	0	0	0
169	2	698	7ff	7ff	7ff	1	0	0	0
170	4	698	2a0	7ff	7ff	0	1	0	0
171	7	698	2a0	7ff	7ff	0	1	0	0
172	8	2a0	7ff	7ff	7ff	1	0	0	0
173	b	6a8	7ff	7ff	7ff	1	0	0	0
174	d	6a8	7ff	7ff	7ff	1	0	0	0
175	e	6ac	7ff	7ff	7ff	1	0	0	0
176	1	6b0	2b8	7ff	7ff	0	1	0	0
177	2	6b0	2b8	7ff	7ff	0	1	0	0
178	4	2bc	7ff	7ff	7ff	1	0	0	0
179	7	2c0	7ff	7ff	7ff	1	0	0	0
180	8	2c0	7ff	7ff	7ff	1	0	0	0
181	b	6c8	7ff	7ff	7ff	1	0	0	0
182	d	6c8	7ff	7ff	7ff	1	0	0	0
183	e	6cc	7ff	7ff	7ff	1	0	0	0
184	0	6d0	2d8	7ff	7ff	0	1	0	0
185	3	6d0	2d8	7ff	7ff	0	1	0	0
186	5	2d8	7ff	7ff	7ff	1	0	0	0
187	6	6e0	7ff	7ff	7ff	1	0	0	0
188	9	6e0	2e8	7ff	7ff	0	1	0	0
189	a	6e0	2e8	7ff	7ff	0	1	0	0
190	c	2ec	7ff	7ff	7ff	1	0	0	0
191	f	2f0	7ff	7ff	7ff	1	0	0	0
192	0	2f0	7ff	7ff	7ff	1	0	0	0
193	3	6f8	7ff	7ff	7ff	1	0	0	0
194	5	6f8	7ff	7ff	7ff	1	0	0	0
195	6	6fc	7ff	7ff	7ff	1	0	0	0
196	9	700	308	7ff	7ff	0	1	0	0
197	a	700	308	7ff	7ff	0	1	0	0
198	c	30c	7ff	7ff	7ff	1	0	0	0
199	f	310	7ff	7ff	7ff	1	0	0	0
200	1	310	7ff	7ff	7ff	1	0	0	0
201	2	718	7ff	7ff	7ff	1	0	0	0
202	4	718	320	7ff	7ff	0	1	0	0
203	7	718	320	7ff	7ff	0	1	0	0
204	8	320	7ff	7ff	7ff	1	0	0	0
205	b	728	7ff	7ff	7ff	1	0	0	0
206	d	728	7ff	7ff	7ff	1	0	0	0
207	e	72c	7ff	7ff	7ff	1	0	0	0
208	1	730	338	7ff	7ff	0	1	0	0
209	2	730	338	7ff	7ff	0	1	0	0
210	4	33c	7ff	7ff	7ff	1	0	0	0
211	7	340	7ff	7ff	7ff	1	0	0	0
212	8	340	7ff	7ff	7ff	1	0	0	0
213	b	748	7ff	7ff	7ff	1	0	0	0
214	d	748	7ff	7ff	7ff	1	0	0	0
215	e	74c	7ff	7ff	7ff	1	0	0	0
216	0	750	358	7ff	7ff	0	1	0	0
217	3	750	358	7ff	7ff	0	1	0	0
218	5	358	7ff	7ff	7ff	1	0	0	0
219	6	760	7ff	7ff	7ff	1	0	0	0
220	9	760	368	7ff	7ff	0	1	0	0
221	a	760	368	7ff	7ff	0	1	0	0
222	c	36c	7ff	7ff	7ff	1	0	0	0
223	f	370	7ff	7ff	7ff	1	0	0	0
224	1	370	7ff	7ff	7ff	1	0	0	0
225	2	778	7ff	7ff	7ff	1	0	0	0
226	4	778	380	7ff	7ff	0	1	0	0
227	7	778	380	7ff	7ff	0	1	0	0
228	8	380	7ff	7ff	7ff	1	0	0	0
229	b	788	7ff	7ff	7ff	1	0	0	0
230	d	788	7ff	7ff	7ff	1	0	0	0
231	e	78c	7ff	7ff	7ff	1	0	0	0
232	0	790	398	7ff	7ff	0	1	0	0
233	3	790	398	7ff	7ff	0	1	0	0
234	5	398	7ff	7ff	7ff	1	0	0	0
235	6	7a0	7ff	7ff	7ff	1	0	0	0
236	9	7a0	3a8	7ff	7ff	0	1	0	0
237	a	7a0	3a8	7ff	7ff	0	1	0	0
238	c	3ac	7ff	7ff	7ff	1	0	0	0
239	f	3b0	7ff	7ff	7ff	1	0	0	0
240	0	3b0	7ff	7ff	7ff	1	0	0	0
241	3	7b8	7ff	7ff	7ff	1	0	0	0
242	5	7b8	7ff	7ff	7ff	1	0	0	0
243	6	7bc	7ff	7ff	7ff	1	0	0	0
244	9	7c0	3c8	7ff	7ff	0	1	0	0
245	a	7c0	3c8	7ff	7ff	0	1	0	0
246	c	3cc	7ff	7ff	7ff	1	0	0	0
247	f	3d0	7ff	7ff	7ff	1	0	0	0
248	1	3d0	7ff	7ff	7ff	1	0	0	0
249	2	7d8	7ff	7ff	7ff	1	0	0	0

250	4	7d8	3e0	7ff	7ff	0	1	0	0
251	7	7d8	3e0	7ff	7ff	0	1	0	0
252	8	3e0	7ff	7ff	7ff	1	0	0	0
253	b	7e8	7ff	7ff	7ff	1	0	0	0
254	d	7e8	7ff	7ff	7ff	1	0	0	0
255	e	7ec	7ff	7ff	7ff	1	0	0	0

Table 11.17: BCID fixed rotary pattern expected outputs

11.7.3 Edge Detection Circuitry

The function of this block is to detect the match of the input signal looking on 3 consecutive BC clock periods to a given pattern. For each successful match found the circuit generates a pulse of duration 1 clock cycle. The effect of this block is that only a single '1' is written into the pipeline for every hit detected according to the match criteria, irrespective of the length of the incoming pulse. The various match pattern on 3 consecutive BC as listed on Table 11.18. With Det_mode at 11 the edge detection circuit enforces 0 at its output independently of the input signal (L0Buffer clearing).

Det_mode(1:0)	Name of Selection Criteria	Hit Pattern (Oldest data bit 1st on the left)	Usage
00	Hit	1XX or X1X or XX1	Detector alignment
01	Level	X1X	Normal Data Taking
10	Edge	01X	Normal Data Taking
11	Clear	None	Special Mode

Table 11.18: Edge Detection Criteria

11.8 Event Buffers

11.8.1 L0BUFFER (Pipeline)

The binary pipeline L0BUFFER is realized with two single port RAM blocks of 320 bits (wide) by 256 bits (length) (164Kbits). The total pipeline length is 512 bits, or 12.8us latency time. Out of the 320 inputs, 256 are for the hit data, 8 are receiving the BC counter value (BCID), and the remaining will be unused (zeroed). When an L0 trigger is received (LCB_IN input), the hit-pattern and BC count from the bits written in the pipeline at a predefined number (Latency register) of clock cycles before, are readout and transmitted to the EvtBuffer. The Latency register is the number of clock cycles representing the L0 latency time. The value of the Latency register is programmable through a register. If a LCB fast command Register_Reset or Logic_Reset is issued, the pointer address generator for the RAM block is reset to address for the write and $010 for the read, while the contents of the pipeline remain unchanged. A description of the L0Buffer arrangement is shown in Figure 11.4.

11.8.2 Hit Counters

An 8 bit counter is attached to each channel at the output of the L0Buffer, that count hits moving from the L0Buffer to the EvtBuffer (therefore controlled by the L0 trigger rate). In this way it is possible to accumulate hit counts, a feature that can be useful in some calibration procedures.

The counting capability for all channels is enabled through the control bit Encount. Counters

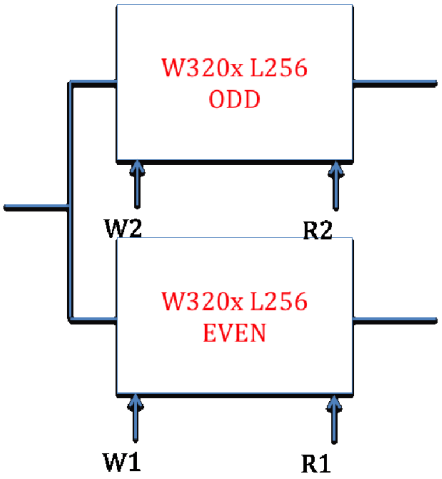

Figure 11.4: L0Buffer (pipeline) arrangement in 2 blocks of 256 320-bits wide words.

values are caught at the time the counters read commands are issued. A single counter read command is able to get counters values for 4 channels. Counters stop when reaching the maximum count ($FF).

All counters are controlled through three fast commands of the LCB protocol listed in Table 11.9, which take effect if Encount is enabled. The Hit Count Reset command forces all counters to zero, the Hit Count Start command makes counting begin and the Hit Count Stop command pauses counting, while preserving the current count values. Note, if Encount is disabled, the Hit Count fast commands have no effect.

11.8.3 EvtBuffer

The readout buffer EvtBuffer is realized by one single port RAM blocks of 320 bits (wide) by 128 bits (length) (41Kbits in total). The buffer length is able to store 128 L0 tagged “events”. With an average L0 event readout rate of 1MHz, the events are stored in the EvtBUFFER for an average duration of 128 microseconds. Out of the 320 inputs, 256 are for the hit data, 8 are for the BC counter value stored in the L0Buffer (BCID), 7 are for the L0tag data, 8 are for the BC counter value at the time of arrival of L0 (known as BC-at-L0 or BCatL0).

11.8.4 EvtBuffer Readout mechanism

The EvtBuffer operation is rather simple to explain: at every occurrence of L0, one event of the EvtBuffer is written in EvtBuffer (1 BC slot). At any occurrence of PR or LP, the event of interest is read out (1 BC slot) and sent to the Cluster Finder block. The identification of the event to readout, within the EvtBuffer memory array, is made with the PRL0ID (or LPL0ID) identifier: these numbers are used as direct pointers (address generators) for reading the EvtBuffer. If PRL0ID and LPL0ID have the same value, they read the same event. To correctly address the event to readout, the PRL0ID (LPL0ID) value has to be equal to the L0tag value that has been written at L0 time. A typical sequence of signals to operate the data extraction from the L0Buffer and EvtBuffer is shown on Figure 11.7.

Because the event readout sequences can occur in parallel and independently of the arrival of the PRL0ID or LPL0ID commands, the respective PRL0ID or LPL0ID numbers are stored in 2 separate FIFOs (LP FIFO and PR FIFO). The size of the FIFOs for the LPL0ID and PRL0ID numbers is 16.

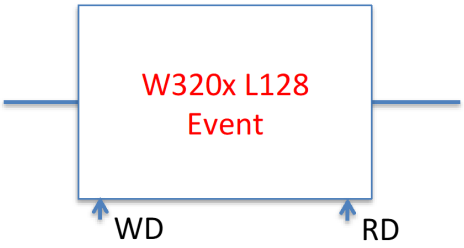

Figure 11.5: EvtBuffer arrangement in 1 block of 128 320-bits wide words.

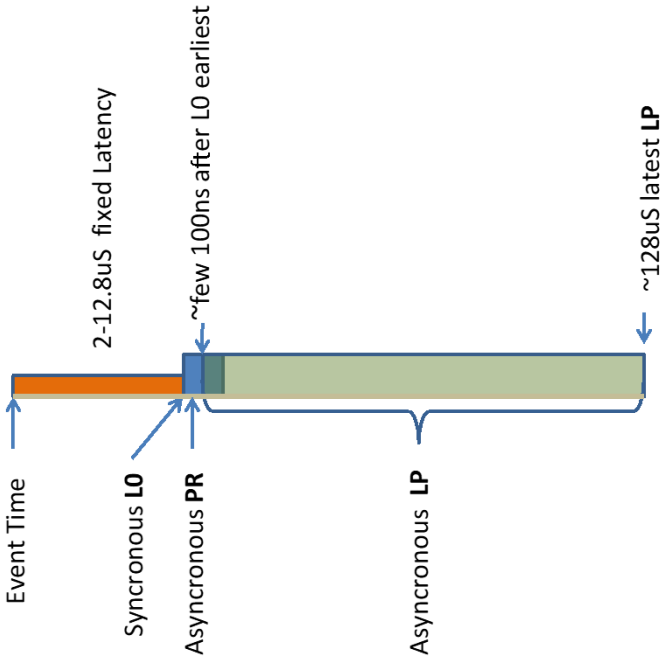

Figure 11.6: L0, PR and LP Latencies

11.8.5 Intermediate FIFO Buffer

The memory blocks of the L0Buffer and EvtBuffer do not support simultaneous write and read in the same clock cycle. In case of writing directly from the L0Buffer to the EvtBuffer, this operation can be continuous for several clock cycles as long as there are contiguous L0 signal. In this case the EvtBuffer Read operation has to be delayed until the write cycles are finished. There is the requirement to minimize the delay time between receiving a PR trigger and sending the corresponding data out of the chip. To keep this delay independent of the number of L0 and hence keep executing the EvtBuffer Read in case of contiguous L0, a small size intermediate FIFO is inserted between the L0Buffer and the EvtBuffer. With this structure and the appropriate control logic, the EvtBuffer Read operation is given priority over writing in the EvtBuffer. When a Read (one clock cycle) occurs, after a LP or PR trigger, if a L0 is at the same time, the event is stored into the intermediate FIFO for one clock cycle. It is transferred to the EvtBuffer after the Read cycle.

11.9 Cluster Finder

11.9.1 Design of the Cluster Finder

The Cluster Finder takes in 256 bits of strip data and reports out 12 bit clusters at 40MHz. A cluster consists of 8 bits of hit address, 3 bits indicating the following 3 strip values and 1 bit

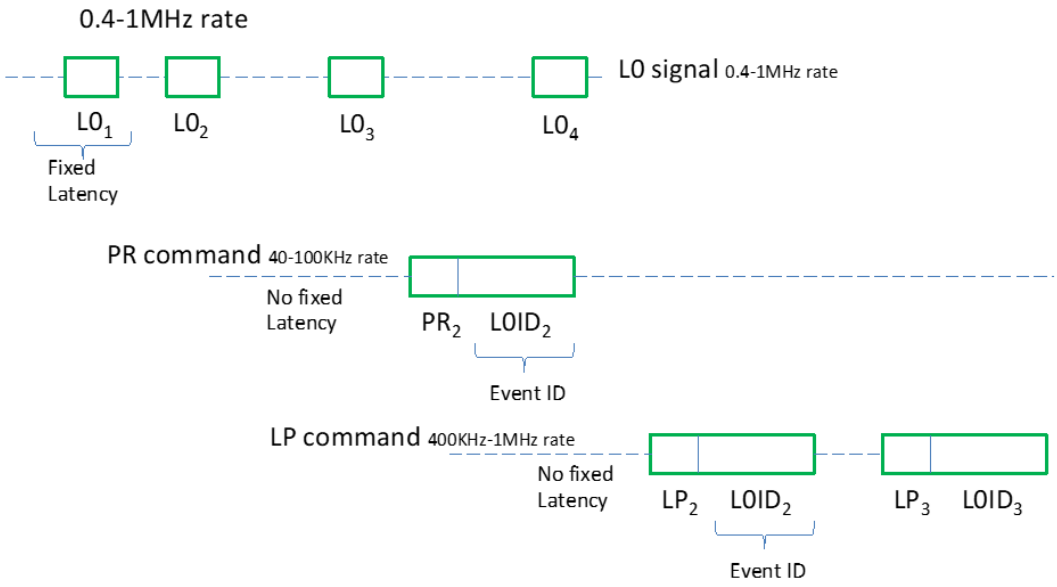

Figure 11.7: Sequence of the internal L0, PR, LP signals used to trigger the physics data readout.

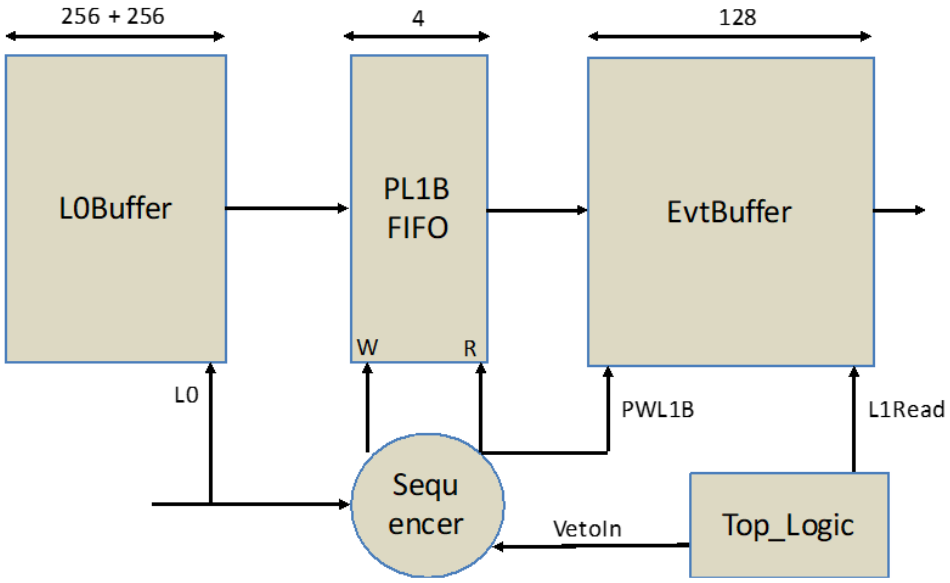

Figure 11.8: PL1B intermediate FIFO insertion between the L0Buffer and the EvtBuffer

denoting whether it is the last cluster or not. The input in_we is the input write enable pin which represents valid input data Data_In. The Data_In is the 256 FE data and it is latched on the positive clock edge when in_we is high. Once it is latched, the Data_In can be safely changed to the next data from the pipeline. The Cluster Finding algorithm is executed on the input data and it reports zero to several clusters of 12 bits. An output pin cluster_we is set high when a valid cluster is sent out. While the Cluster Finder is operating on a 256 data input, it flags out CF_busy as 1 to the preceding pipeline. The last_cluster is enabled high when the Cluster Finder outputs the last cluster detected in the 256 bit strip data.

There is a flow control builtin, as the serialization of the output packets is slower than the cluster finder. When necessary, the Xoff goes high and the cluster finder temporarily stops. A high Xoff signal halts the Cluster transmission and a low Xoff signal resumes the Cluster

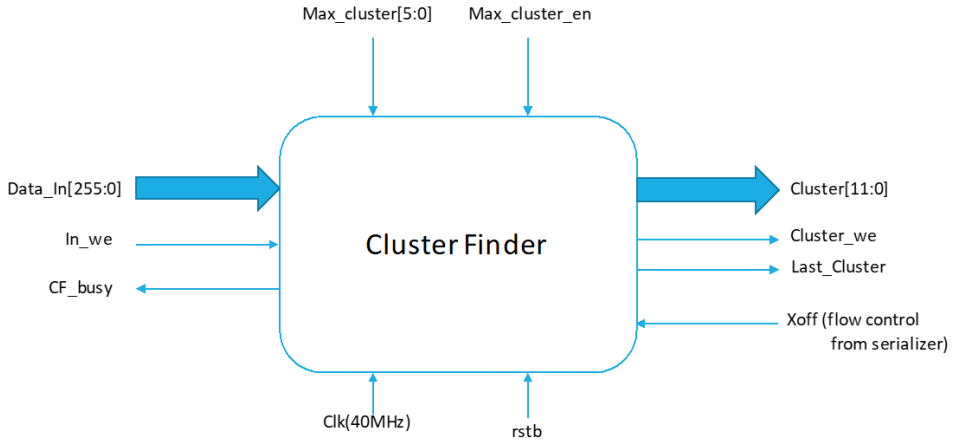

Figure 11.9: Cluster Finder

transmission. This is controlled by the cluster finder FIFO in the readout block.

1 bit (Last Cluster) (1 bit)	8 bits Address of the Hit (8 bits)	Following 3 strip values (3 bits)

Table 11.19: 12-bit Cluster data

11.9.2 Interaction of the two 128 strips Cluster Finders to cover 256 strips

Each Cluster Finder sub-block treats 128 strips of the same strip row of the detector. The Cluster Finder deals with strip data as odds and evens. Two identical Cluster Finder sub-blocks (A or C) are required to treat the 256 strips. The rearrangement block inside the Cluster Finder takes in 256 bits of input data and separates it into 2 banks of 128 bits called Odd and Even banks, to group together bits of adjacent channels in a strip row. The odd-numbered channels are grouped to the odd data bank and the even-numbered channels are grouped to the even data bank.
dataOdd [i] = dataIn[2*i + 1] i=0,1,2,...127
dataEven[i] = dataIn[2*i] i=0,1,2,...127
The 2 sets of 128 bit data are sent to the CF128_odd and CF128_even blocks which are enabled alternately by a state machine. The 2 banks report out clusters one bank at a time in an alternate fashion to avoid bias to any 1 bank. The Cluster Finder always start reporting clusters from the odd bank first, then the even bank, and continues the process until it has reported out all clusters. When the odd bank is empty, the Cluster Finder starts reporting out clusters from the even bank one clock cycle later. When both the banks are empty, the Cluster Finder reports out a reserved 12 bit No Cluster Output. The Max_cluster_enable and Max_cluster[5:0] bits can be used to limit the number of clusters produced by the Cluster Finder. The absolute maximum number of clusters per event is 64 (corresponding to 16 packets and approximately 6.8us transmission time).

11.9.3 No Cluster Output Case

For Physics packets with no hits/clusters, the ABCStar outputs $3FE in the first cluster and $7FF in the next 3 clusters.

$3FE is a special cluster value which is physically impossible and therefore does not appear in real data.

The derivation of $3FE is: it represents strip address 127 with hits in the two following strips,

which do not physically exist (because strip 127 is the final strip on a strip sensor). The most significant bit of the 12-bit cluster, the Last Cluster flag, is also set because this No Cluster value is the last cluster. The following 3 clusters will contain the Empty Cluster value $7FF. See table 11.24 for details of cluster encoding.

11.9.4 Cluster Finder Timing

The Cluster Finder latches in the 256 bit strip data during the positive 40MHz clock edge when the input write signal (in_we) is enabled. The Cluster Finder algorithm is first executed on the odd bank, and the hit address along with the 3 next strip values is obtained in 1 clock cycle. In the next clock cycle, this cluster is checked for the last cluster, and Cluster Finder algorithm is executed in parallel on the even bank.

So, the Cluster Finder reports out the first cluster 2 clock cycles (50ns) after the input data latch, for the case when the odd bank is not empty. When the odd bank is empty, the Cluster Finder reports out the first cluster after 3 clock cycles (75ns) from the even bank. The clusters are reported out every clock after the first cluster unless an Xoff signal is asserted from the Readout Block. For the no cluster case, the special 12 bit output 12'h3FE is sent after 3 clock cycles (75ns).

Pin Name	Function	Active High/Low	Direction
Clk	40 MHz Clock.	Clock	Input
rstb	System Reset	Active Low	Input
Data_in [255:0]	256 bit Strip data	Active High	Input
in_we	Input Data Valid Signal	Active High	Input
Xoff	Output Data Flow Control Signal	Active High	Input
Cluster[11:0]	12 bit cluster (8 bit hit address, 3 bit strip values, 1 bit last cluster)	Active High	Output
Cluster_we	Output Data Valid Signal	Active High	Output
Last_cluster	Indicates last cluster	Active High	Output
Max_cluster_enable	Enables the maximum number of clusters per event	Active High	Input
Max_cluster[5:0]	Maximum number of clusters per event	Decimal 1 to 63	Input
CF_busy	Input Data Flow Control Signal	Active High	Output

Table 11.20: Pin Configuration for Cluster Finder

11.9.5 Interaction with the Readout Block

The transmission of the clusters from the Cluster Finder to the Readout is controlled by the Xoff signal. When the input data is latched and the first cluster is generated (after 2 or 3 cycles), the Cluster Finder checks the Xoff line to determine whether the Readout is ready to accept clusters. Xoff being low signals that the Readout is ready to accept clusters. The Cluster Finder then begins the transmission of clusters to the Readout Block by writing them into the ClusterFinder FIFO. The Readout Block then applies the prioritization described in Table 11.21 to determine when to serialize the clusters found in the ClusterFinder FIFO. If this FIFO becomes almost full, the Readout Block asserts an active high Xoff signal to the Cluster Finder to halt the writing of clusters until the readout serialiser catches up.

11.10 Readout Circuitry

The readout circuitry is responsible for building data packets with the hit patterns coming from the Cluster Finder blocks or from data in the registers to be read, including the HPR register. Each packet is transmitted by the fast 160Mb/s serializer. For physics data, the header is presented at the output, and then the consecutive bits forming the cluster bytes follow until the data packet is complete. All packets belonging to the same event are sent out consecutively, but with the possibility of insertion of different packet types according to the priority mechanism. For the register read-back, a different header is presented at the output, and then the register bit values follow. HPR packets are also constructed by getting the HPR register data and attaching a specific header. A controller (Top_Logic) defines the priority and the order in which packets are formatted and then sent out serially.

TYP	Nickname	Priority order	FIFO size at Readout block interface
High Priority Register	HPR	1	4
Priority Readout	PR	2	4 - both PR and LP are stored in the same ClusterFinder FIFO
Low Priority	LP	3	4 - both PR and LP are stored in the same ClusterFinder FIFO
Register Read	RR	4	4

Table 11.21: Priority order and FIFO size of the readout system

11.10.1 Detailed Description: Interaction with the Cluster Finder (LP and PR data)

The description of the readout system follows the elements of Figure 11.10. The following description is done for the case of LP trigger signal. It applies equally well for the operation with a PR trigger signal. The interaction between LP trigger and PR trigger in the Readout is discussed in a subsequent paragraph. As soon as an LP readout is authorized, the Readout obtains from the higher control level logic the LP_Data_Start signal, and from the EvtBuffer the L0tag value and the BCID value. (The Data_Busy signal is set to one.) The 16 bits header for physics data is assembled and the transmission at 160 MHz starts as soon as possible. During the time of the header transmission, the Cluster Finder has performed the first cluster finder action. When the first cluster data is valid (12 bits, made of 8 bits of address, 3 bits of bitmap and the Last_cluster bit) the Cluster data is sent to the Readout with the Write_en signal. At the end of the header transmission, the Readout sends the first cluster data. During the transmission of any cluster data, if the Last_cluster bit of the current cluster is 0, the next cluster data is presented to the Readout with the Cluster_we signal. The Readout sets the Xoff output bit high to freeze the cluster search in Cluster Finder, until the Readout is able to process it. If the LastCluster bit of the current cluster is 1, the serialisation process stops after the current cluster last bit is transmitted.

The following description is done for the case of LP trigger signal. It applies equally well for the operation with a PR trigger signal. The interaction between LP trigger and PR trigger in the Readout is discussed in a subsequent paragraph. As soon as an LP readout is authorized, the Readout obtains from the higher control level logic the LP_Data_Start signal, and from the EvtBuffer the L0tag value and the BCID value. (The Data_Busy signal is set to one.) The 16 bits header for physics data is assembled and the transmission at 160 MHz starts as soon as possible. During the time of the header transmission, the Cluster Finder has performed the first cluster finder action. When the first cluster data is valid (12 bits, made of 8 bits of

address, 3 bits of bitmap and the Last_cluster bit) the Cluster data is sent to the Readout with the Write_en signal. At the end of the header transmission, the Readout sends the first cluster data. During the transmission of any cluster data, if the Last_cluster bit of the current cluster is 0, the next cluster data is presented to the Readout with the Cluster_we signal. The Readout sets the Xoff output bit high to freeze the cluster search in Cluster Finder, until the Readout is able to process it. If the LastCluster bit of the current cluster is 1, the serialisation process stops after the current cluster last bit is transmitted.

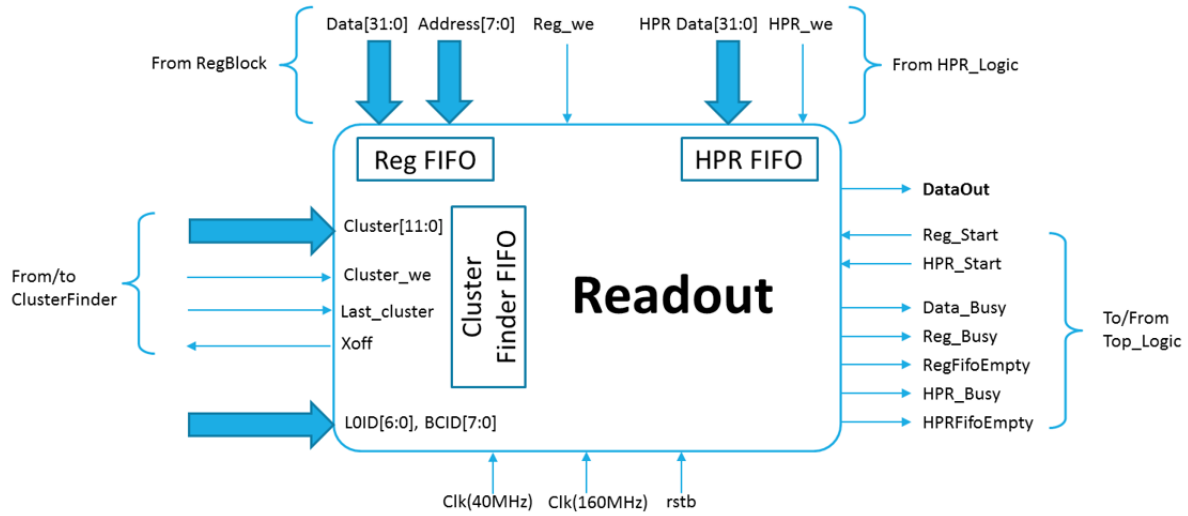

Figure 11.10: Readout logic blocks showing the core packet builder

11.10.2 Detailed Description: Interaction between PR and LP in the Readout

PR and LP triggers are using the same Cluster Finder block. The difference is in the priority given to the PR triggered events. If a PR (or LP) trigger is received, in the absence of LP (resp. PR) trigger, the Cluster Finder and Readout mechanisms are identical to what is described above. If a PR trigger signal is received when the Readout is already processing an LP triggered event, the process of sending packets of the PR event is appended at the end of the existing LP event transmission. Only when the PR trigger event buffer is empty, and the last cluster of the last PR event has been found, can packets of pending LP events be processed.

11.10.3 Register Readback

All internal 32 bits registers contents can be read out through a 68 bits packet format.

Sending a command to read a given register will result in the transmission of one “Register packet” that contains the register identification and the 32 bits of data.

However, the physics packets transmissions have some level of priority, in particular the PR packets. Because of this, at reception of the read register command, the register data is internally stored into an 8 position Register Data FIFO, and the transmission occurs only when some conditions are met. We define 2 cases for the transmission of register packets, independent of when the read register command has been received:

First case (default): the register packet(s) are transmitted as soon as there are no pending LP or PR events in the LP or PR FIFO of the chip.

Second case: because it is possible that events are queued for a long time in the chip, and because some of the registers may contain critical data (like status bits), register readback can

be expedited using "RRforce" can be sent: in such a case the oldest register data pending inside the Register Data FIFO is transmitted after the current LP or PR event packet transmission is finished, and if there is no pending PR events. To allow RRforce to be used, RRmode[1:0] must be set to binary 10, as described in table 11.34.

11.10.4 HPR Packets

The contents of the High Priority Register (HPR, address $3F) are transmitted periodically to provide a snapshot of the state of the ABCStar, especially of the status of the LCB link, as a debugging aid. HPR packets are essentially unsolicited Register Reads.

Format:

HPR packets have the same format as Register Read packets, except for these differences:

1. HPR packets have their own TYP code

Priority of HPR packets and interactions with Physics data:

The ABCStar readout gives the highest priority to HPR packets, followed by physics and other packets. As HPR packet transmission occurs periodically (1ms rate), there are enough time intervals left to transmit other packets.

HPR packets have their own dedicated packet FIFO, as shown in figure 11.10.

11.10.5 Sending of HPR packets and timing

The sending of HPR packets is governed by the passage of time and changes of LCB Lock status. This behaviour can be modified by three control bits, StopHPR and TestHPR in register $00 and MaskHPR.

11.10.5.1 Behaviour in the initial 500us after a reset

In the 500us period following these types of reset: power up reset, external hard reset (RST_b pin), Register Reset and Logic Reset:

- Changes of LCB Lock status during this initial period do not cause HPR packets to be sent
- Setting TestHPR to 1 sends an HPR packet immediately; then a 1ms timer is started (see next section).
- Setting StopHPR to 1 sends an HPR packet immediately; the HPR timer is stopped. See the next section. (Note that by design, one initial HPR packet must always be sent, so the chip sends that initial HPR packet in response to the StopHPR.)
- In the absence of the events above (TestHPR or StopHPR), once 500us have elapsed since a reset, an HPR packet is sent; then a 1ms timer is started (see next section).

Note: setting MaskHPR to 1 during this initial period does not affect the sending of packets.

11.10.5.2 Behaviour after the first HPR is sent

Following a reset, after the first HPR packet has been sent, the sending of HPR packets changes. Now HPR packets are sent every 1ms or when the LCB Lock status changes. In addition, that behaviour can be modified by setting the TestHPR, StopHPR and MaskHPR bits, as explained in the next sections.

11.10.5.3 After the first HPR, if the timer is running

If the HPR timer is running (StopHPR has not been set to 1):

- If LCB lock is lost or regained, if MaskHPR is 0 (not masked), an HPR packet is sent immediately and the HPR 1ms timer is cleared and restarted.
- If TestHPR is set to 1, if MaskHPR is 0 (not masked), an HPR packet is sent immediately and the HPR 1ms timer is cleared and restarted.
- If LCB lock is lost or regained, or TestHPR is set to 1, but MaskHPR is 1 (events are masked), then either of these events has no effect: no HPR packet is sent and the HPR timer continues counting.
- Setting StopHPR to 1 stops the HPR timer (see next section).
- In the absence of the events above, once 1ms has elapsed, an HPR packet is sent; then the HPR 1ms timer is cleared and restarted.

11.10.5.4 After the first HPR, if the timer is stopped

If the HPR timer is stopped (StopHPR was set to 1):

- If LCB lock is lost, if MaskHPR is 0 (not masked), an HPR packet is sent immediately and the HPR 1ms timer is cleared and restarted. From this point, periodic HPR packets resume (see previous section).
- If TestHPR is set to 1, if MaskHPR is 0 (not masked), an HPR packet is sent immediately and the HPR 1ms timer is cleared and restarted. From this point, periodic HPR packets resume (see previous section).
- If LCB lock is lost, or TestHPR is set to 1, but MaskHPR is 1 (events are masked), then either of these events has no effect: no HPR packet is sent and the HPR timer is not restarted.
- Setting StopHPR to 1 again has no effect (the timer is already stopped).

11.10.5.5 Configuration of HPR behaviour

To sum up how to achieve specific outcomes: DAQ can control how HPR packets are sent using 3 control bits, TestHPR and StopHPR (in register \$00) and MaskHPR (in register \$20), as follows:

- To receive an HPR packet immediately: set TestHPR to 1. Assuming MaskHPR is 0 (not masked), this acts as a one-time pulse, as if the LCB_Locked bit had changed.
- To not receive periodic HPR packets: set StopHPR to 1. Note that a subsequent change of LCB lock status will restart the periodic sending of HPR packets.
- To not receive HPR packets when LCB_Locked changes: set MaskHPR to 1. TestHPR will also be ignored. Note that if StopHPR has not been set to 1, the periodic sending of HPR packets will continue.
- To not receive **any** HPR packets: first set MaskHPR to 1, then set StopHPR to 1. Then no further HPR packets will be sent.
- To make HPR packets resume, after stopping and masking them: set MaskHPR to 0 (to allow TestHPR to be perceived), then set TestHPR to 1. This resumes both the periodic HPR packets and the HPR packets resulting from changes to LCB_Locked. Alternatively, send a Logic Reset or Register Reset fast command.

Note that setting StopHPR to 0 has no effect (in particular, it does not resume periodic sending of HPR packets - see just above for how to resume).

Setting TestHPR to 0 also has no effect.

11.11 Readout Packet Formats

In ABCStar the output format has a 68 fixed bit length readout packet format. A packet always starts with the HEADER 111 (binary) and ends with a stop bit of value 0. It is possible to transmit back-to-back packets. There are only three possible types of packets from the ABCStar (LP, PR, HPR and register reads) and a complete list is presented in table 11.22.

TYPE code	Meaning
0001	PR packet
0010	LP packet
0100	ABC register read packet
0111	Reserved to HCC
1000	Reserved to HCC
1011	Reserved to HCC
1101	ABC HPR register packet
1110	Reserved

Table 11.22: TYPE descriptor

A complete packet comparison bet LP/PR, HPR and read register type of packets is presented in table 11.23.

11.11.1 Physics packets: LP or PR

A packet in case of physics data is made of a:

- 3 bits preamble (start bits)
- TYPE indicator which is either LP or PR packet type
- FlagBit as status
- The respective L0tag event
- BCID[2:0] and its parity check
- 4 clusters information, 12 bits each
- stop bit (always at 0)

In case of events with less than 4 clusters, the 'empty cluster byte' (value = $7FF) is used.

In case of events with no hits/clusters, the "no cluster byte' (value = $3FE) is used.

In case of events with more than 4 clusters, a first packet is formed with the framing and the Physics Header (16 bits) followed by the 4 cluster bytes. Then other packets are formed with the framing and the same Physics Header (16 bits) followed by 4 cluster bytes or empty cluster bytes, until all clusters for one event are transmitted. A "LAST_CLUSTER" bit value set at one marks the last cluster for a given event. A descriptive table of a cluster is presented in 11.24.

frame bit	LP/PR packet type	Register Read packet type	HPR packet type
67	start bit = 1	start bit = 1	start bit = 1
66	start bit = 1	start bit = 1	start bit = 1
65	start bit = 1	start bit = 1	start bit = 1
64	Type[3] = 0	Type[3] = 0	Type[3] = 1
63	Type[2] = 0	Type[2] = 1	Type[2] = 1
62	Type[1] = 0 (PR) or 1 (LP)	Type[1] = 0	Type[1] = 0
61	Type[0] = 1 (PR) or 0 (LP)	Type[0] = 0	Type[0] = 1
60	FlagBit (1 bit)	RegisterAddress[7]	HPR check bit = 1
59	L0tag[6]	RegisterAddress[6]	HPR check bit = 1
58	L0tag[5]	RegisterAddress[5]	HPR check bit = 1
57	L0tag[4]	RegisterAddress[4]	K2 pending
56	L0tag[3]	RegisterAddress[3]	SEU counter [7]
55	L0tag[2]	RegisterAddress[2]	SEU counter [6]
54	L0tag[1]	RegisterAddress[1]	SEU counter [5]
53	L0tag[0]	RegisterAddress[0]	SEU counter [4]
52	BCID[2]	SEU counter [3]	SEU counter [3]
51	BCID[1]	SEU counter [2]	SEU counter [2]
50	BCID[0]	SEU counter [1]	SEU counter [1]
49	xor(BCID[7:0])	SEU counter [0]	SEU counter [0]
48	Cluster1_lastcluster	Register contents[31]	LCB_S(15)
47	Cluster1[10]	Register contents[30]	LCB_S(14)
46	Cluster1[9]	Register contents[29]	LCB_S(13)
45	Cluster1[8]	Register contents[28]	LCB_S(12)
44	Cluster1[7]	Register contents[27]	LCB_S(11)
43	Cluster1[6]	Register contents[26]	LCB_S(10)
42	Cluster1[5]	Register contents[25]	LCB_S(9)
41	Cluster1[4]	Register contents[24]	LCB_S(8)
40	Cluster1[3]	Register contents[23]	LCB_S(7)
39	Cluster1[2]	Register contents[22]	LCB_S(6)
38	Cluster1[1]	Register contents[21]	LCB_S(5)
37	Cluster1[0]	Register contents[20]	LCB_S(4)
36	Cluster2_lastcluster	Register contents[19]	LCB_S(3)
35	Cluster2[10]	Register contents[18]	LCB_S(2)
34	Cluster2[9]	Register contents[17]	LCB_S(1)
33	Cluster2[8]	Register contents[16]	LCB_S(0)
32	Cluster2[7]	Register contents[15]	LCB_SCmd_Err
31	Cluster2[6]	Register contents[14]	LCB_ErrCnt_Ovfl
30	Cluster2[5]	Register contents[13]	LCB_Decode_Err
29	Cluster2[4]	Register contents[12]	LCB_Locked
28	Cluster2[3]	Register contents[11]	ADC_dat(11)
27	Cluster2[2]	Register contents[10]	ADC_dat(10)
26	Cluster2[1]	Register contents[9]	ADC_dat(9)
25	Cluster2[0]	Register contents[8]	ADC_dat(8)
24	Cluster3_lastcluster	Register contents[7]	ADC_dat(7)
23	Cluster3[10]	Register contents[6]	ADC_dat(6)
22	Cluster3[9]	Register contents[5]	ADC_dat(5)
21	Cluster3[8]	Register contents[4]	ADC_dat(4)
20	Cluster3[7]	Register contents[3]	ADC_dat(3)
19	Cluster3[6]	Register contents[2]	ADC_dat(2)
18	Cluster3[5]	Register contents[1]	ADC_dat(1)
17	Cluster3[4]	Register contents[0]	ADC_dat(0)
16	Cluster3[3]	chipID[3]	chipID[3]
15	Cluster3[2]	chipID[2]	chipID[2]
14	Cluster3[1]	chipID[1]	chipID[1]
13	Cluster3[0]	chipID[0]	chipID[0]
12	Cluster4_lastcluster	OR of all SEU bits	OR of all SEU bits
11	Cluster4[10]	FlagBit	FlagBit
10	Cluster4[9]	PRFIFO almost full	PRFIFO almost full
9	Cluster4[8]	PRFIFO empty	PRFIFO empty
8	Cluster4[7]	LPFIFO almost full	LPFIFO almost full
7	Cluster4[6]	LPFIFO empty	LPFIFO empty
6	Cluster4[5]	RegFIFO overflow	RegFIFO overflow
5	Cluster4[4]	RegFIFO almost full	RegFIFO almost full
4	Cluster4[3]	RegFIFO empty	RegFIFO empty
3	Cluster4[2]	ClusterFIFO overflow	ClusterFIFO overflow
2	Cluster4[1]	ClusterFIFO almost full	ClusterFIFO almost full
1	Cluster4[0]	ClusterFIFO empty	ClusterFIFO empty
0	1 stop bit = 0	1 stop bit = 0	1 stop bit = 0

Table 11.23: Packet format comparison

Last Cluster Flag	Cluster Address	Next Strips Pattern
1	8	3

Table 11.24: Cluster Byte definition

11.11.2 Register reads packets

For a register readback packet, which contains the register identification and register contents (status, flags, SEU detection, configuration, input patterns, analogue bias setting, etc.), a packet is formed with the 4 bits framing (3 bits preamble and 1 bit trailer), the 16-bit "Register Header" part containing the data type and register identification, followed by the payload made of the the 32-bit register contents, and 16 bits containing status bits.

All the read packets contain the same status bits in the 16 last bits of the 48 bits payload, as defined in Table 11.25.

The 10 first status bits are the value of the flags attached to the FIFOs containing pending data to be serialised or pending event identifiers. There values are loaded at the time of the start of the packet serialisation. The 4 last bits are the wired ABCStar chipID. In more detail:

- chipID is the chip physical address.
- OR of all SEU bits is high when a voting on the triplication logic has been detected.
- FlagBit will depend on the selected EN_out_decoder[3:0] register value. Refer to table 11.31.
- PRFIFO Full is set to 1 when all entries have been written.
- PRFIFO Empty is set to 1 when all entries have been read.
- LPFIFO Full is set to 1 when all entries have been written.
- LPFIFO Empty is set to 1 when all entries have been read.
- RegFIFO OVFL is set to 1 when the FIFO has overflown, meaning that it was already full and then another write took place, overwriting the oldest data.
- RegFIFO Full is set to 1 when all entries have been written.
- RegFIFO Empty is set to 1 when all entries have been read.
- Cluster OVFL is set to 1 when the FIFO has overflown, meaning that it was already full and then another write took place, overwriting the oldest data.
- Cluster Full is set to 1 when all entries have been written.
- Cluster Empty is set to 1 when all entries have been read.

11.11.3 HPR packets

An HPR packet is similar to a register read packet.

11.12 Beam Crossing Counter

This is an 8-bit binary counter which is incremented on every clock cycle. This counter is zeroed by either hardware reset, a software reset, or the BCR signal issued from the LCB input protocol and its decoding circuit. The BC counter value is entered in the pipeline at each clock cycle and transferred to the readout buffer at the time of a L0. It is also directly entered in the EvtBuffer at the time of the L0. It is expected that the difference of BCID values between

frame bit	Value
16	chipID[3]
15	chipID[2]
14	chipID[1]
13	chipID[0]
12	OR of all SEU bits
11	FlagBit
10	PRFIFO almost full
9	PRFIFO empty
8	LPFIFO almost full
7	LPFIFO empty
6	RegFIFO overflow
5	RegFIFO almost full
4	RegFIFO empty
3	ClusterFIFO overflow
2	ClusterFIFO almost full
1	ClusterFIFO empty

Table 11.25: Register Read Status bits

entering the pipeline and entering the EvtBuffer is constant once the pipeline latency has been fixed.

11.13 LCB Command Decoder

In ABCStar there are two classes of commands (CMD bit of the LCB protocol): fast commands (6-bit command format) and register commands (55-bit or 20-bit command format). Fast commands are global and have a direct effect on the chips operation: they are used to resynchronize the BC and Trigger counters, and eventually they return the chip in predefined default states (Register_Reset or Logic_Reset). Register commands are global or addressable commands to execute Write or Read operations into the internal registers. The read register commands should not interfere with the data taking operation, however there may be limitations if such commands are received when the chip is in data taking mode (see also the HCCStar operation).

11.13.1 Fast commands

The 6 bits commands are received on the 4 BC frame format of the LCB protocol. In the case of the ABCStar chip, different reset commands have been defined, i.e. the Register_Reset, BC Reset commands, SEU registers reset. It is expected that these commands will be sent to the chip at regular intervals during periods of time when no triggers signals will be sent to the chip. The purpose of these commands is to perform controlled resets of the chip. The digital test and the analogue calibration pulse signals are also generated by fast commands to control precisely the synchronization to the BC number:

- CalPulse : Generate the analogue calibration pulse, 400ns wide (16BC). The polarity is controlled by the register CalPulsePolarity. The analogue calibration pulse is enabled only if register CalPulseEnable is enabled.
- DigitalPulse : Generate a test signal at the input of the pipeline (through the Channel Mask Register). The digital test signal is enabled only if register TestPulseEnable is enabled.

11.13.2 Register commands

These are long packets that enable the operation of the chip to be controlled by setting bits in registers. Only the addressed chips will act on the packet, unless the address sent equals '1111', in which case all chips will act on the packet. All chips that receive the packet must decode it, even if they do not act on it. This is to avoid un-addressed chips erroneously decoding parts of the data field as the start of packets. Write and Read register commands can be sent to the chip during normal data taking (ie. at the same time as L0, PR or LP inputs), however this should be done with precaution as it may affect the chip settings or produce additional data added to the data flow toward the HCCStar. The transmission of registers data packets produced by read commands are taking the lowest priority as compared to the PR or LP packets transmissions: the register content addressed by the Read command are sent out only if no PR or LP packets are pending. A mode is set through the RRforce bit to enforce one read register transmission in front of pending LP packets. Write commands executions can be switched-off by setting bit WriteDisable, to prevent a chip to be accidentally reconfigured.

The register commands are received through the LCB protocol. The commands are presented in the tables below (Table 11.26 and Table 11.27) in the form of the sequences of the significant bits in the LCB bits streams.

Field 1, 1 bit , HCC/ABC	Field 2, 4 bits HCC, ChipID	Field 3, 1 bit, (R/W)	Field 4, 4 bits ABC, ChipID	Field 5, 8 bits , Register address	Field 6, Spare 4/1 bits	Field 7, (32 bits), Data	Description
1	cccc	0 = W	aaaa	'h00	nnnn	32'hddddddddd	Special Register
1	cccc	0 = W	aaaa	'h0F-'h01	nnnn	32'hddddddddd	Analogue and DCS registers
1	cccc	0 = W	aaaa	'h17-'h10	nnnn	32'hddddddddd	Mask Registers
1	cccc	0 = W	aaaa	'h1F-'h18	nnnn	32'hddddddddd	Pattern input registers
1	cccc	0 = W	aaaa	'h2F-'h20	nnnn	32'hddddddddd	Configuration registers
1	cccc	0 = W	aaaa	'h3F-'h30	nnnn	32'hddddddddd	Status registers
1	cccc	0 = W	aaaa	'h5F-'h40	nnnn	32'hddddddddd	LSB Trim DAC registers
1	cccc	0 = W	aaaa	'h67-'h60	nnnn	32'hddddddddd	MSB Trim DAC registers
1	cccc	0 = W	aaaa	'h6F-'h68	nnnn	32'hddddddddd	Calibration Enable registers

Table 11.26: Register Commands (Write)

Field 1, 1 bit, HCC/ABC	Field 2, '1'4 bits HCC , ChipID	Field 3, 1 bit, (R/W)	Field 4, 4 bits ABC, ChipID	Field 5, 8 bits , Register address	Field 6, Spare 4/1 bits	Field 7, (32 bits), Data	Description
1	cccc	1=R	aaaa	'h00	n	-	Special Register

1	cccc	1=R	aaaa	‘h0F-’h01	n	-	Analogue and DCS registers
1	cccc	1=R	aaaa	‘h17-’h10	n	-	Mask Registers
1	cccc	1=R	aaaa	‘h1F-’h18	n	-	Pattern input registers
1	cccc	1=R	aaaa	‘h2F-’h20	n	-	Configuration registers
1	cccc	1=R	aaaa	‘h3F-’h30	n	-	Status registers
1	cccc	1=R	aaaa	‘h5F-’h40	n	-	LSB Trim DAC registers
1	cccc	1=R	aaaa	‘h67-’h60	n	-	MSB Trim DAC registers
1	cccc	1=R	aaaa	‘h6F-’h68	n	-	Calibration Enable registers
1	cccc	1=R	aaaa	‘hBF-’h80	n	-	”Hit Counters registers”

Table 11.27: Register Commands (Read)

Legends:

- n = don’t care value.
- aaaa = 4 bits ABCID chip address (MSB bit first)
- cccc = HCCID code
- 32’hddddddddd = 32 bits values for registers (MSB bit first)
- Field 2: This is the 4 bit reserved for the HCC ChipID. If it has the special code ‘1110’ the command is aborted. Otherwise this field is ignored by ABCStar chips.
- Field 3: This bit is zero if command is to Write in register, 1 if command is to Read register.
- Field 4: This is the 4 bit of the ABCStar ChipID. ‘1111’ is used as the broadcast address.
- Field 5: The register addresses are distributed in ranges of 16 consecutive addresses per part of the chip. There can be unused bits per register and unused addresses in the range. Precise definition of the register content per address will be part of each block functional description.
- Field 6: This field holds 1 to 4 unused bits : they are here to adapt the command length to the segmentation into fixed length frames occurring in the LCB encoding mechanism.
- Field 7: This field holds the 32 bits data that is to be written into the selected register.

Registers banks are separated in groups :

- ANALOG and DCS : Write and Read registers, default setting at reset. Write protected by the WriteDisable register.
- INPUT : Mask bits (also test pattern injection), Write and Read. Write protected by the WriteDisable register.
- CONFIGURATION : Configuration bits, Write and Read, Preset value at reset. Write protected by the WriteDisable register.
- STATUS and SEU : Read only registers. The STATUS register at address $3F is defined as the high priority Status Register. SEU registers are reset by the OR of Register_Reset and the specific SEU Reset command.

- TrimDAC and Calibration : Write and Read registers, default setting at reset. Write protected by the WriteDisable register.
- Hit-Counters: Read registers which hold the 8-bit counter information of the hit counters.

11.13.3 SEU Protection

The logic has been fully triplicated, including triplicated clocks using a tree voter scheme for maximum protection. Nonetheless, the crossection will not be zero, as the combinatorial A/B/C paths have not been physically spaced constrained in the chip, only the A/B/C flip-flops by 10 um distance.

11.14 Registers Map

11.14.1 Special Register, address : $00 (1 register of 32 bits)

Register Name	SCReg
ADDR	0x00
bit 31	0
bit 30	1
bit 29	0
bit 28	0
bit 27	1
bit 26	0
bit 25	1
bit 24	0
bit 23	0
bit 22	1
bit 21	0
bit 20	1
bit 19	0
bit 18	0
bit 17	0
bit 16	0
bit 15	0
bit 14	1
bit 13	0
bit 12	0
bit 11	1
bit 10	0
bit 9	1
bit 8	0
bit 7	0
bit 6	ADCReset
bit 5	LCBErrCntClr
bit 4	eFuseL
bit 3	TestHPR
bit 2	StopHPR
bit 1	WriteDisable
bit 0	RRforce
SEUbit	scREGSEU
Reset Value (hex)	4A50 4A00

Table 11.28: Special Register

See table 11.28. Bit Functions :

- RRforce : When set, the oldest pending “Read Register” packet is transmitted after the current LP or PR event packet transmission is finished, and if there is no pending PR events. The RRforce bit is internally reset after the execution.
- WriteDisable : if set this bit prevents write commands on registers other than $00 to be active (protection against spurious commands).
- StopHPR : When set at one interrupts the periodic transmission of the HPR register. The StopHPR bit is internally reset after the execution.

- TestHPR : When set it provides one pulse acting as an LCB_Locked bit being false. This bit is to test the HPR periodic packet transmission. The TestHPR bit is internally reset after the execution.
- eFuseL : When set it provides one pulse that copies the 24 programmed eFuse bits into the eFuse register (Status Register at address $32). The eFuseL bit is internally reset after the execution.
- LCBErrCntClr: When set to one, the LCB Error Counter (Status Register at address $34) is cleared. If the LCB_ErrCnt_Ovfl flag is set (in the High Priority Register at address $3F), it is also cleared. The LCBErrCntClr is internally reset after execution.
- ADCReset: resets the ADC

11.14.2 Analog and DCS Registers, addresses : $01 to $03

See table 11.29 for the analog and DCS Registers.

See the Front-end section for the bias under control by each bits group. The default sets all bias currents to the minimum, the discriminator voltage (BVT) to the maximum, the calibration pulse delay and amplitude to zero or minimum, the MUX output is not enabled, and the regulators output value tuning are not active. The regulator outputs are set to the maximum.

See the monitoring ADC section to configure the ADC.

Bit Functions :

- ADCS1
  - BVREF[4:0]
  - BIREF[4:0]
  - B8BREF[4:0]
  - BTRANGE[4:0]
  - BVT[7:0]
  - DIS_CLKS[2:0]: allows to disable one of the 7 possible clocks (clk40MA clk40MB, clk40MC, clk40MV, clk160MA, clk160MB or clk160MC). It is impossible to disable more than one clock at a time and should only be done during production testing. It is necessary to enable register bit DIS_CLKS_EN which is located in another register bank for security. Check table 11.30.
  - LCB_SelfResetEnable: This was added as a backdoor to the LCB decoder. This self resets the LCB decoder when the LCB decoder error reaches saturation (register LCB_ErrCount_Thr[7:0]).
- ADCS2
  - STR_DEL_R[1:0]
  - STR_DEL[5:0]
  - COMBIAS[4:0]
  - BCAL[8:0]
  - IDLEPATTERN[3:0]: To facilitate HCCSTAR deserializers' life and to add transitions on the 160Mbps data output line an idle pattern has been introduced. This can be configured to 4'b0000 to revert back to ABCSTARV0 behavior.
  - enGlitchFilter_40MA/B/C/V/ADC: Triplicated glitch filters were added on the 40M pads. This is to avoid glitches on the clock line coming from HCCSTAR. Caution: the 40MHz clock phase can and will change with regards to the 160M inside the chip. New calibration will be necessary after enabling this. The usefulness and to know if it is baseline to enable the glitchFilter is to be determined during SEE run. There is no glitch filter for the 160M pads. If one glitch filter is enabled, all glitch filters have to be enabled for the chip to work properly.

  - ringOscRadMonitoring_enable: ringOscRadMonitoring_enable enables the radiation monitoring ring oscillator circuit. This is to be done from time to time during radiation and during normal operation when the chip is not being used for data taking. Disable during normal operation. The ring oscillator counter counts the ring oscillator's clock pulses and appears in register ringOscRadMonitoring_counts[31:0]. Counter operation is controlled using the following existing fast LCB commands. When ringOscRadMonitoring_enable is set to 1, these fast commands are repurposed to act on the ring oscillator counter instead of the hit counters. The new effect of the commands is:
    * FMCD_ABC_HIT_RST: reset the ring oscillator counter value to zero
    * FMCD_ABC_HIT_START: begin counting ring oscillator pulses
    * FMCD_ABC_HIT_STOP: stop counting ring oscillator pulses - this freezes the counter at its current value

- ADCS3
  - ADC_Bias[3:0]
  - ADC_Ch[3:0]
  - ADC_Enable: enabled the ADC
  - BTMUXDEC[3:0]: uses decimal encoding. Refer to table 11.3.
  - BTMUXD: Activated the analog test mux.
  - A_S_DEC[4:0]: controls the analog LDO.
  - A_LOW: Lowers the output voltage of the analog LDO.
  - A_EN_CTRL: Enables the analog LDO. At zero the LDO is at its maximum voltage.
  - D_S_DEC[4:0]: controls the digital LDO.
  - D_LOW: Lowers the output voltage of the analog LDO.
  - D_EN_CTRL: Enables the analog LDO. At zero the LDO is at its maximum voltage.
  - EN_out_decoder[3:0] configures the flagBit in the 68-bit packets. Refer to table 11.31.

11.14.3 Input (Mask) Registers, addresses : $10 to $17 (8 registers of 32 bits)

The Input (Mask) Registers bits are used to mask the channel when bit TM[0] is clear. Channels are numbered from 0 to 255 in the same order as for the readout. The Input (Mask) Registers bits inject a fixed pattern or a test pulse sequence in the L0 pipeline if bit TM[0] is set (bit 16 of register $20). See table 11.32.

11.14.4 Configuration Registers, address range $20 to $2F is reserved (16 registers of 32 bits).

Address Range $20 to $21 is reserved for configuration registers. See table 11.33.

Bit Functions :

- Register $20 :
  - TestPulseEnable : When set enables the digital test pulse functions at the input of the pipeline
  - EnCount : when set enables the counters at the end of the L0Buffer (pipeline). When reset the counters are disabled (counting stopped).
  - MaskHPR : When set it prevents HPR packets from being transmitted when the synchronization status of the LCB link changes (masking the LCB_Locked bit).
  - PR_enable is the bit to enable (1) or disable (0) the transmission of data originating from the PR Triggers.
  - LP_enable is the bit to enable (1) or disable (0) the transmission of data originating from the LP Triggers.

Register Name	ADCS1	ADCS2	ADCS3
ADDR	$01	$02	$03
bit 31	LCB_SelfResetEnable	ringOscRadMonitoring_enable	EN_out_decoder[3]
bit 30	DIS_CLKS[2]	enGlitchFilter_40MADC	EN_out_decoder[2]
bit 29	DIS_CLKS[1]	enGlitchFilter_40MV	EN_out_decoder[1]
bit 28	DIS_CLKS[0]	enGlitchFilter_40MC	EN_out_decoder[0]
bit 27	BVT(7)	enGlitchFilter_40MB	D_EN_CTRL
bit 26	BVT(6)	enGlitchFilter_40MA	D_LOW
bit 25	BVT(5)	IDLEPATTERN[3]	D_S_DEC[4]
bit 24	BVT(4)	IDLEPATTERN[2]	D_S_DEC[3]
bit 23	BVT(3)	IDLEPATTERN[1]	D_S_DEC[2]
bit 22	BVT(2)	IDLEPATTERN[0]	D_S_DEC[1]
bit 21	BVT(1)	BCAL(8)	D_S_DEC[0]
bit 20	BVT(0)	BCAL(7)	A_EN_CTRL
bit 19	BTRANGE(4)	BCAL(6)	A_LOW
bit 18	BTRANGE(3)	BCAL(5)	A_S_DEC[4]
bit 17	BTRANGE(2)	BCAL(4)	A_S_DEC[3]
bit 16	BTRANGE(1)	BCAL(3)	A_S_DEC[2]
bit 15	BTRANGE(0)	BCAL(2)	A_S_DEC[1]
bit 14	B8BREF(4)	BCAL(1)	A_S_DEC[0]
bit 13	B8BREF(3)	BCAL(0)	BTMUXD
bit 12	B8BREF(2)	COMBIAS(4)	BTMUXDEC[3]
bit 11	B8BREF(1)	COMBIAS(3)	BTMUXDEC[2]
bit 10	B8BREF(0)	COMBIAS(2)	BTMUXDEC[1]
bit 9	BIREF(4)	COMBIAS(1)	BTMUXDEC[0]
bit 8	BIREF(3)	COMBIAS(0)	ADC_Enable
bit 7	BIREF(2)	STR_DEL(5)	ADC_Ch(3)
bit 6	BIREF(1)	STR_DEL(4)	ADC_Ch(2)
bit 5	BIREF(0)	STR_DEL(3)	ADC_Ch(1)
bit 4	BVREF(4)	STR_DEL(2)	ADC_Ch(0)
bit 3	BVREF(3)	STR_DEL(1)	ADC_Bias(3)
bit 2	BVREF(2)	STR_DEL(0)	ADC_Bias(2)
bit 1	BVREF(1)	STR_DEL_R(1)	ADC_Bias(1)
bit 0	BVREF(0)	STR_DEL_R(0)	ADC_Bias(0)
SEUbit	ADCS1SEU	ADCS2SEU	ADCS3SEU
Reset Value (hex)	0FF0 0000	0180 0000	0000 0000

Table 11.29: DCS registers

CLOCKS	DIS_CLKS_EN	DIS_CLKS[2]	DIS_CLKS[1]	DIS_CLKS[0]	DIS_CLKS[3:0] (dec)
clk40A	1	0	0	1	1
clk40B	1	0	1	0	2
clk40C	1	0	1	1	3
clk40V	1	1	0	0	4
clk40ADC	ADCEnable				
clk160A	1	1	0	1	5
clk160B	1	1	1	0	6
clk160C	1	1	1	1	7

Table 11.30: Disable triplicated clocks list

- RRmode[1:0] controls the Read Register function. Disabling the read register transmission does not prevent the internal FIFO to fill up, and may result in the FIFO full/overflow flags going high. See table 11.34.
- TM(1:0) : these bits control the functions of the Input (Mask) Registers bits. Refer to table 11.16.
- TestPattEnable : if zero the digital test pulse command generate 1 BC long pulse per unmasked channels. If one, the 8 bits TestPatt1(3:0) and TestPatt2(3:0) are used to create the test pulse patterns applied to Unmask channels or Mask channels.
- TestPatt1(3:0) are used to create the test pulse patterns applied to Unmask channels.
- TestPatt2(3:0) are used to create the test pulse patterns applied to Mask channels.

EN_out_decoder	EN_out_decoder[3:0] (dec)
EN_LCB_SCmd_Err	0
EN_LCB_ErrCnt_Ovfl	1
EN_LCB_Decode_Err	2
EN_LCB_Locked	3
EN_PRFIFO_OVFL	4
EN_PRFIFO_AlmostFull	5
EN_PRFIFO_Empty	6
EN_LPFIFO_OVFL	7
EN_LPFIFO_AlmostFull	8
EN_LPFIFO_Empty	9
EN_RegFIFO_OVFL	10
EN_RegFIFO_AlmostFull	11
EN_RegFIFO_Empty	12
EN_Cluster_OVFL	13
EN_Cluster_AlmostFull	14
EN_Cluster_Empty	15

Table 11.31: EN_out_decoder (flagBit)

Register Name	MaskInput0	MaskInput1	MaskInput2	MaskInput3	MaskInput4	MaskInput5	MaskInput6	MaskInput7
ADDR	$10	$11	$12	$13	$14	$15	$16	$17
bit 31	ch31	ch63	ch95	ch127	ch159	ch191	ch223	ch255
bit 30	ch30	ch62	ch94	ch126	ch158	ch190	ch222	ch254
bit 29	ch29	ch61	ch93	ch125	ch157	ch189	ch221	ch253
bit 28	ch28	ch60	ch92	ch124	ch156	ch188	ch220	ch252
bit 27	ch27	ch59	ch91	ch123	ch155	ch187	ch219	ch251
bit 26	ch26	ch58	ch90	ch122	ch154	ch186	ch218	ch250
bit 25	ch25	ch57	ch89	ch121	ch153	ch185	ch217	ch249
bit 24	ch24	ch56	ch88	ch120	ch152	ch184	ch216	ch248
bit 23	ch23	ch55	ch87	ch119	ch151	ch183	ch215	ch247
bit 22	ch22	ch54	ch86	ch118	ch150	ch182	ch214	ch246
bit 21	ch21	ch53	ch85	ch117	ch149	ch181	ch213	ch245
bit 20	ch20	ch52	ch84	ch116	ch148	ch180	ch212	ch244
bit 19	ch19	ch51	ch83	ch115	ch147	ch179	ch211	ch243
bit 18	ch18	ch50	ch82	ch114	ch146	ch178	ch210	ch242
bit 17	ch17	ch49	ch81	ch113	ch145	ch177	ch209	ch241
bit 16	ch16	ch48	ch80	ch112	ch144	ch176	ch208	ch240
bit 15	ch15	ch47	ch79	ch111	ch143	ch175	ch207	ch239
bit 14	ch14	ch46	ch78	ch110	ch142	ch174	ch206	ch238
bit 13	ch13	ch45	ch77	ch109	ch141	ch173	ch205	ch237
bit 12	ch12	ch44	ch76	ch108	ch140	ch172	ch204	ch236
bit 11	ch11	ch43	ch75	ch107	ch139	ch171	ch203	ch235
bit 10	ch10	ch42	ch74	ch106	ch138	ch170	ch202	ch234
bit 9	ch9	ch41	ch73	ch105	ch137	ch169	ch201	ch233
bit 8	ch8	ch40	ch72	ch104	ch136	ch168	ch200	ch232
bit 7	ch7	ch39	ch71	ch103	ch135	ch167	ch199	ch231
bit 6	ch6	ch38	ch70	ch102	ch134	ch166	ch198	ch230
bit 5	ch5	ch37	ch69	ch101	ch133	ch165	ch197	ch229
bit 4	ch4	ch36	ch68	ch100	ch132	ch164	ch196	ch228
bit 3	ch3	ch35	ch67	ch99	ch131	ch163	ch195	ch227
bit 2	ch2	ch34	ch66	ch98	ch130	ch162	ch194	ch226
bit 1	ch1	ch33	ch65	ch97	ch129	ch161	ch193	ch225
bit 0	ch0	ch32	ch64	ch96	ch128	ch160	ch192	ch224
SEUbit	MT0SEU	MT1SEU	MT2SEU	MT3SEU	MT4SEU	MT5SEU	MT6SEU	MT7SEU
Reset Value (hex)	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000

Table 11.32: INPUT (MASK) REGISTERS

- TestPulse Enable : at zero it prevents any spurious activation of a digital test pulse at the Pipeline inputs (SEU mitigation). Test Pulses are allowed only if this bit is set to one.
- CurrDrive(3:0) : set current drive of DAT outputs (DAT outputs are active at powerup or RegReset).
- CalPulseEnable : When set enables the analogue pulse functions at the input of channels
- CalPulsePolarity swaps the 16BC wide analog calibration pulse polarity
- Latency(8:0) sets the latency in the L0 pipeline in number of BC clocks (default at reset is 400 BC (10us))

Register Name	CREG0	CREG1
ADDR	$20	$21
bit 31	Latency(8)	ReadoutTimeoutEnable
bit 30	Latency(7)	LCB_ErrCount_Thr(7)
bit 29	Latency(6)	LCB_ErrCount_Thr(6)
bit 28	Latency(5)	LCB_ErrCount_Thr(5)
bit 27	Latency(4)	LCB_ErrCount_Thr(4)
bit 26	Latency(3)	LCB_ErrCount_Thr(3)
bit 25	Latency(2)	LCB_ErrCount_Thr(2)
bit 24	Latency(1)	LCB_ErrCount_Thr(1)
bit 23	Latency(0)	LCB_ErrCount_Thr(0)
bit 22	CalPulsePolarity	DIS_CLKS_EN
bit 21	CalPulseEnable	V0ReadoutMode
bit 20	CurrDriv(2)	DOFUSEADDR[4]
bit 19	CurrDriv(1)	DOFUSEADDR[3]
bit 18	CurrDriv(0)	DOFUSEADDR[2]
bit 17	TestPatt2(3)	DOFUSEADDR[1]
bit 16	TestPatt2(2)	DOFUSEADDR[0]
bit 15	TestPatt2(1)	Max_Cluster_Enable
bit 14	TestPatt2(0)	Max_Cluster(5)
bit 13	TestPatt1(3)	Max_Cluster(4)
bit 12	TestPatt1(2)	Max_Cluster(3)
bit 11	TestPatt1(1)	Max_Cluster(2)
bit 10	TestPatt1(0)	Max_Cluster(1)
bit 9	TestPattEnable	Max_Cluster(0)
bit 8	TM(1)	Det mode(1).
bit 7	TM(0)	Det mode(0).
bit 6	RRmode(1)	DTESTOUTSEL[6]
bit 5	RRmode(0)	DTESTOUTSEL[5]
bit 4	LP_Enable	DTESTOUTSEL[4]
bit 3	PR_Enable	DTESTOUTSEL[3]
bit 2	MaskHPR	DTESTOUTSEL[2]
bit 1	EnCount	DTESTOUTSEL[1]
bit 0	TestPulseEnable	DTESTOUTSEL[0]
SEUbit	CFG0SEU	CFG1SEU
Reset Value (hex)	C810_0000	7F80_0002

Table 11.33: CONFIGURATION REGISTER CREG0 and CREG1

- Register $21 :
  - DTESTOUTSEL[6:0]: added digital test output to monitor internal signals. Refer to table 11.35 and 11.36 for an extensive list.
  - Det_mode(1:0) are bits controlling the Input Register detection criteria. Refer to table 11.18.
  - Max_Cluster(5:0) : if the bit Max_Cluster_Enable is set, these bits value fixes the maximum number of clusters sent per event. Minimum allowed is 0 (no clusters are send).
  - Max_Cluster_Enable : at one limits the number of clusters to the value represented by Max_Cluster(5:0). At zero the number of packets can reach the maximum possible number of clusters per LP or PR event ie. 64.
  - DoFuse bits are used to program (fuse) the eFuse cells, using position 0 to 23. The encoding is decimal, where 0 means no efuse bit selected. The value to be fused can be read from the status registers before being fused. Refer to table 11.37.
  - V0ReadoutMode: Modifies the packet format to be compatible with V0 mode when enabled. Refer to table 11.38.
  - DIS_CLKS_EN: enables the possibility to disable clocks.
  - LCB_ErrCount_Thr(15:0) is the LCB error count threshold. If the number of number of LCB synchronization and decoder errors (LCB_ErrCount, Status Register $34) exceeds this threshold, the status bit LCB_ErrCnt_Ovfl gets set in the High Priority Register ($3F).
  - ReadoutTimeoutEnabled: There is a fixed timeout for the readout block. This will make a self reset on the packet building block in case the state machine hangs for whatever reason.

V0 Register Read	V1 Register Read	V0 High Priority Register	V1 High Priority Register

3 start bits: 111	3 start bits: 111	3 start bits: 111	3 start bits: 111
Type: 0100	Type: 0100	Type: 1101	Type: 1101
Register address (8 bits)	Register address (8 bits)	Register address (8 bits)	”HPR check bits”: 111, ”K2 pending”, SEU counter[7:4]
0000	SEU counter [3:0]	0000	SEU counter [3:0]
Register contents (32 bits)	Register contents (32 bits)	Register contents (32 bits)	Register contents (32 bits)
Status bits (16 bits)	Status bits (16 bits)	Status bits (16 bits)	Status bits (16 bits)
1 stop bit = 0	1 stop bit = 0	1 stop bit = 0	1 stop bit = 0

Table 11.38: V0 and V1 packets comparison

11.14.5 Status Registers, address range $30 to $3E is reserved (15 registers of 32 bits)

See tables 11.39 and 11.40.

- All signals with the suffix SEU: These registers will be ’1’ if the correction mechanism has kicked-in. It means that one of the A/B/C branches had a different value than the other two branches. These flags are only cleared by sending the fast command SEUReset.
- PRFIFO, LPFIFO, L0HoldFIFO, clusterFIFO, HPRFIFO and RegFifo status signals are also available.
- PR_Bad and LP_Bad are reset-less and saturation free counters which are incremented when bad PR or LP requests are detected.
- ABCSTARVER is a static identifier, fixed to 89 (hex)
- eFusedValue[23:0] holds the efuse value. Necessary to load it by enabling the eFuseL registers in the SCREG.
- K2_pending: high is a K2 is pending in the LCB protocol
- ADCMeasurementReady is high if a new ADC sample is ready which is in ADC_dat[11:0]. This flag is cleared by reading register STAT3.
- A carbon-copy of the ADC configuration is also in this register to facilitate production testing.
- SEUcount[7:0] is incremented when a voter makes a correction in the SCREG, ADCS and CREG. This counter is resetless and does not saturate.
- LCB_SCmd_Err is high if an error in the LCB has been detected.
- LCB_ErrCnt_Ovfl is high if the LCB_ErrCount[7:0] has overflowed. The saturation point is set by the register LCB_ErrCount_Thr[7:0].
- The value2eFuse[23:0] is used to cross-check the corrected selected efuse selected by register DOFUSEADDR[4:0].
- ringOscRadMonitoring_counts[31:0] is the output of a ring oscillator which will allow to monitor the radiation degradation.

11.14.6 High Priority Register (HPR), address $3F (1 register of 32 bits)

This register content is transmitted automatically by means of the HPR. It can be read like any other register by receiving a Register Read command. See table 11.41.

- ADC_dat(11:0) are the current outputs of the ADC. By default (after power up or a Register_Reset command the ADC is ON and the internally regulated digital voltage is selected).
- LCB_Locked: LCB circuit flag at one when the LCB circuit is correctly synchronized with the input stream on the LCB_IN inputs. It is at zero when synchronization is lost. This flag reflects the real-time status of the synchronization.

RRmode[1:0]	Meaning
00	Read Register disabled
01	Read Register if no pending LP/PR
10	One Read Register if no PR pending, when RRforce is enabled
11	Read Register if no pending LP/PR

Table 11.34: RRmode settings

DIGITAL TEST OUT	
Signal	Sel[6:0] (dec)
1'b0	127
1'b0	126
1'b0	125
1'b0	124
1'b0	123
1'b0	122
1'b0	121
1'b0	120
1'b0	119
1'b0	118
1'b0	117
1'b0	116
1'b0	115
1'b0	114
&(enableGFBC)	113
Xoff	112
SEUcount[1]	111
SEUcount[0]	110
Top_Logic_SEU	109
HPR_State_SEU	108
ReadOut_SEU	107
PacketBuilder_SEU	106
L0_SEU	105
EvtBuf_SEU	104
lcb_see_err_bus_o	103
SEUFlagsORed	102
incrSEUCount	101
Flag_Bit	100
LPbadPacket	99
PRbadPacket	98
StopHPR	97
MaskHPR	96
TestHPR	95
ABCFastCmdPulse	94
RBreadPulse	93
RBbusy	92
LCB_frame_raw[15]	91
LCB_frame_raw[10]	90
LCB_frame_raw[7]	89
LCB_frame_raw[5]	88
LCB_frame_raw[3]	87
LCB_frame_raw[0]	86
LCB_fast_cmd_valid	85
LCB_ErrCount[0]	84
LCB_Decode_Err	83
LCB_ErrCnt_Ovfl	82
LCB_SCmd_Err	81
RBinit	80
RBsload	79
RBrnw	78
clk_ringosc_o	77
PBResetb	76
(HPR_Start—LP_ADDR_FIFO_ReadEnable—PR_ADDR_FIFO_ReadEnable—Reg_Start)	75
Reg_Start	74
CountStart — CountStop — CountReset	73
regReadPush	72
BusyForPhysics	71
HPR_Start	70
BusyForRegHPR	69
PushHPR	68
K2Pending	67
CF_busy_fromCF	66
Cluster_we	65
L0A	64

Table 11.35: Digital test output list

- LCB_Decode_Err: LCB circuit flag set when one of the following errors has occurred: invalid symbol (outside of the defined set of symbols), parity error or bad nibble (0000 or 1111). For the ABCStarV1, this value is not latched (this was a design error).
- LCB_ErrCnt_Ovfl: this LCB error flag becomes one when the number of LCB synchronization

DIGITAL TEST OUT	
Signal	Sel[6:0] (dec)
LP_ADDR_FIFO_ReadEnable	63
PR_ADDR_FIFO_ReadEnable	62
data_fromEvtBuf_Typ	61
data_fromEvtBuf_Valid	60
ClusterFifoOverflow	59
ClusterFifoFull	58
ClusterFifoAlmostFull	57
ClusterFifoEmpty	56
RegFifoOverflow	55
RegFifoFull	54
RegFifoAlmostFull	53
RegFifoEmpty	52
HPRFifoOverflow	51
HPRFifoFull	50
HPRFifoAlmostFull	49
HPRFifoEmpty	48
LP_ADDR_FIFO_overflow	47
LP_ADDR_FIFO_full	46
LP_ADDR_FIFO_almostFull	45
LP_ADDR_FIFO_empty	44
PR_ADDR_FIFO_overflow	43
PR_ADDR_FIFO_full	42
PR_ADDR_FIFO_almostFull	41
PR_ADDR_FIFO_empty	40
L0HOLD_ADDR_FIFO_empty	39
L0HOLD_ADDR_FIFO_overflow	38
digitalTestPulse	37
calPulse	36
CalPulseTo	35
CountStart	34
CountStop	33
CountReset	32
BCID[7]	31
BCID[5]	30
BCID[1]	29
BCID[0]	28
RegResetb	27
LogResetb	26
SEUresetb	25
SCMDResetb	24
LCB_bcr	23
hardRstb	22
hardRstbPresync	21
FCLRN	20
FSETP	19
BCtV	18
BCtA	17
BCtB	16
BCtC	15
BCtADC	14
L1DataIn	13
R3DataIn	12
RSTB_gf	11
abcup_gf	10
powerUpRstb_gf	9
chipID_gf[3]	8
chipID_gf[2]	7
chipID_gf[1]	6
chipID_gf[0]	5
PRLP	4
ADCDataReady	3
LCB_Locked	2
VDD	1
GND	0

Table 11.36: Digital test output list (continuation)

and decoder errors (LCB_ErrCount, Status Register $34) exceeds the LCB error count threshold (LCB_ErrCount_Thr, Configuration Register $26). This flag persists until it is cleared by writing a '1' to the bit LCBErrCntClr in Register $00. It is not cleared when an HPR packet is sent or this register ($3F) is read.

- LCB_SCmd_Err : LCB circuit flag set when an error takes place during a Slow Command LCB sequence. For the ABCStarV1, this value is not latched (this was a design error).
- LCB_S(15:0) : these bits are the 16 160Mb/s bits tracked during the 4 BC period that is identified by the LCB circuit to synchronize the LCB symbols. This is also known as the "raw LCB frame" as these are the bits received before any decoding takes place.

DOFUSEADDR[4:0]	DOFUSE BIT
0	none
1	0
2	1
3	2
4	3
5	4
6	5
7	6
8	7
9	8
10	9
11	10
12	11
13	12
14	13
15	14
16	15
17	16
18	17
19	18
20	19
21	20
22	21
23	22
24	23
25	none
26	none
27	none
28	none
29	none
30	none
31	none

Table 11.37: DoFuseAddr table

Register Name	STAT0	STAT1	STAT2	STAT3
ADDR	$30	$31	$32	$33
bit 31	ReadOutSEU	0	ABCSTARVER[7]	K2_pending
bit 30	HPRCountSEU	0	ABCSTARVER[6]	RegFifoOverflow
bit 29	HPRStateSEU	0	ABCSTARVER[5]	RegFifoFull
bit 28	TopLSEU	PRFIFOOverflow	ABCSTARVER[4]	RegFifoAlmostFull
bit 27	1'b0	PRFIFOFull	ABCSTARVER[3]	RegFifoEmpty
bit 26	SCRegSEU	PRFIFOAlmostFull	ABCSTARVER[2]	ADCMeasurementReady
bit 25	CR47SEU	PRFIFOEmpty	ABCSTARVER[1]	ADC_dat(11)
bit 24	CR43SEU	LPFIFOOverflow	ABCSTARVER[0]	ADC_dat(10)
bit 23	CR39SEU	LPFIFOFull	eFusedValue(23)	ADC_dat(9)
bit 22	CR35SEU	LPFIFOAlmostFull	eFusedValue(22)	ADC_dat(8)
bit 21	CR31SEU	LPFIFOEmpty	eFusedValue(21)	ADC_dat(7)
bit 20	CR27SEU	L0HoldFifoOverflow	eFusedValue(20)	ADC_dat(6)
bit 19	CR23SEU	L0HoldFifoEmpty	eFusedValue(19)	ADC_dat(5)
bit 18	CR19SEU	ClusterFifoOverflow	eFusedValue(18)	ADC_dat(4)
bit 17	CR15SEU	ClusterFifoFull	eFusedValue(17)	ADC_dat(3)
bit 16	CR11SEU	ClusterFifoAlmostFull	eFusedValue(16)	ADC_dat(2)
bit 15	CR7SEU	ClusterFifoEmpty	eFusedValue(15)	ADC_dat(1)
bit 14	CR3SEU	HPRFifoOverflow	eFusedValue(14)	ADC_dat(0)
bit 13	MT7SEU	HPRFifoFull	eFusedValue(13)	BTMUXD
bit 12	MT6SEU	HPRFifoAlmostFull	eFusedValue(12)	BTMUXDEC[3]
bit 11	MT5SEU	HPRFifoEmpty	eFusedValue(11)	BTMUXDEC[2]
bit 10	MT4SEU	EvtIDLatchSEU	eFusedValue(10)	BTMUXDEC[1]
bit 9	MT3SEU	L0SEU	eFusedValue(9)	BTMUXDEC[0]
bit 8	MT2SEU	PktBldSEU	eFusedValue(8)	ADC_Enable
bit 7	MT1SEU	PR_Bad[3]	eFusedValue(7)	ADC_Ch(3)
bit 6	MT0SEU	PR_Bad[2]	eFusedValue(6)	ADC_Ch(2)
bit 5	ADCS3SEU	PR_Bad[1]	eFusedValue(5)	ADC_Ch(1)
bit 4	ADCS2SEU	PR_Bad[0]	eFusedValue(4)	ADC_Ch(0)
bit 3	ADCS1SEU	LP_Bad[3]	eFusedValue(3)	ADC_Bias(3)
bit 2	1'b0	LP_Bad[2]	eFusedValue(2)	ADC_Bias(2)
bit 1	CFG1SEU	LP_Bad[1]	eFusedValue(1)	ADC_Bias(1)
bit 0	CFG0SEU	LP_Bad[0]	eFusedValue(0)	ADC_Bias(0)
SEUbit	no	no	no	no
Reset Value (hex)	0000_0000	0000_0000	8900_0000	0000_0000

Table 11.39: STATUS REGISTER

11.14.7 TrimDAC Registers, addresses: $40 to $67, 40 registers

Each 32 bits register in the range $40 to $5F contains the 4 LSB bits of the TrimDAC for 8 channels. In such a way the 32-bit register contains the value for 8 channels. Each 32 bits register in the range $60 to $6F contains the MSB bit of the TrimDAC for 32 channels.

Note: one SEU flag bit is generated for a group of 4 registers. For the 40 TrimDAC registers there are 10 SEU bit names: CR3SEU CR7SEU CR11SEU CR15SEU CR19SEU CR23SEU CR27SEU CR31SEU CR35SEU CR39SEU. See table 11.42, 11.43, 11.44, 11.45, 11.46, 11.47, 11.48, 11.49, 11.50 and 11.51.

11.14.8 Calibration Enable Registers ($68 to $6F, 8 registers)

Each 32 bits register contains 1 bit per channel enabling the calibration pulse. See tables 11.52 and 11.53.

Note : one SEU flag bit is generated for a group of 4 registers. For the 8 TrimDAC registers there are 2 SEU bit names : CR43SEU CR47SEU.

11.14.9 Hit Counters Registers ($80 to $BF, 64 registers)

Each 32 bits register contains the 8 bit counts of the Hit Counters for 4 channels. See table 11.54.

Note : No SEU flag is provided, the registers are not protected against SEU, as these registers are used outside of physics. When used inside physics, they may be used as pipeline SEU counters if there are no physics hits entering the L0buffer (by masking all channels).

Register Name	STAT4	STAT5	STAT6
ADDR	$34	$35	$36
bit 31	SEUCount[7]	1'b0	ringOscRadMonitoring_counts[31]
bit 30	SEUCount[6]	1'b0	ringOscRadMonitoring_counts[30]
bit 29	SEUCount[5]	1'b0	ringOscRadMonitoring_counts[29]
bit 28	SEUCount[4]	1'b0	ringOscRadMonitoring_counts[28]
bit 27	SEUCount[3]	1'b0	ringOscRadMonitoring_counts[27]
bit 26	SEUCount[2]	1'b0	ringOscRadMonitoring_counts[26]
bit 25	SEUCount[1]	1'b0	ringOscRadMonitoring_counts[25]
bit 24	SEUCount[0]	1'b0	ringOscRadMonitoring_counts[24]
bit 23	0	value2eFuse(23)	ringOscRadMonitoring_counts[23]
bit 22	0	value2eFuse(22)	ringOscRadMonitoring_counts[22]
bit 21	0	value2eFuse(21)	ringOscRadMonitoring_counts[21]
bit 20	0	value2eFuse(20)	ringOscRadMonitoring_counts[20]
bit 19	0	value2eFuse(19)	ringOscRadMonitoring_counts[19]
bit 18	LCB_SCmd_Err	value2eFuse(18)	ringOscRadMonitoring_counts[18]
bit 17	LCB_ErrCnt_Ovfl	value2eFuse(17)	ringOscRadMonitoring_counts[17]
bit 16	LCB_Decode_Err	value2eFuse(16)	ringOscRadMonitoring_counts[16]
bit 15	LCB_SCmd_ErrCount(7)	value2eFuse(15)	ringOscRadMonitoring_counts[15]
bit 14	LCB_SCmd_ErrCount(6)	value2eFuse(14)	ringOscRadMonitoring_counts[14]
bit 13	LCB_SCmd_ErrCount(5)	value2eFuse(13)	ringOscRadMonitoring_counts[13]
bit 12	LCB_SCmd_ErrCount(4)	value2eFuse(12)	ringOscRadMonitoring_counts[12]
bit 11	LCB_SCmd_ErrCount(3)	value2eFuse(11)	ringOscRadMonitoring_counts[11]
bit 10	LCB_SCmd_ErrCount(2)	value2eFuse(10)	ringOscRadMonitoring_counts[10]
bit 9	LCB_SCmd_ErrCount(1)	value2eFuse(9)	ringOscRadMonitoring_counts[9]
bit 8	LCB_SCmd_ErrCount(0)	value2eFuse(8)	ringOscRadMonitoring_counts[8]
bit 7	LCB_ErrCount(7)	value2eFuse(7)	ringOscRadMonitoring_counts[7]
bit 6	LCB_ErrCount(6)	value2eFuse(6)	ringOscRadMonitoring_counts[6]
bit 5	LCB_ErrCount(5)	value2eFuse(5)	ringOscRadMonitoring_counts[5]
bit 4	LCB_ErrCount(4)	value2eFuse(4)	ringOscRadMonitoring_counts[4]
bit 3	LCB_ErrCount(3)	value2eFuse(3)	ringOscRadMonitoring_counts[3]
bit 2	LCB_ErrCount(2)	value2eFuse(2)	ringOscRadMonitoring_counts[2]
bit 1	LCB_ErrCount(1)	value2eFuse(1)	ringOscRadMonitoring_counts[1]
bit 0	LCB_ErrCount(0)	value2eFuse(0)	ringOscRadMonitoring_counts[0]
SEUbit	no	no	no
Reset Value (hex)	0000_0000	0000_0000	0000_0000

Table 11.40: STATUS REGISTER 2

11.15 Chip ID

The ABCStar chip address field is 4 bits, different from the ABCD case, where it was 6 bits (and only 4 bits transmitted). To enable a chip to be individually addressed four inputs ID(3:0) will be used to implement a geographical addressing scheme. This is because there may be up to 16 chips to be addressed on each hybrid. These inputs will be wire bonded to a unique set of logic levels for each chip. This set of logic levels will form a geographical address that will enable individual chips on the hybrid to be addressed. Each address input has an internal pull-up. The address "1111" (15) is reserved for global addressing (all chips respond).

11.16 Chip Initialization and Configuration

The following sequence of instructions should normally be sent to the chip after power-up

- 1) Send command to load the configuration registers with the appropriate settings.
- 2) Send a command to load the mask registers
- 3) Send a series of commands to load the DAC register/s and Delay registers

The chip will now be in a state to receive L0 and PR or LP trigger commands and send data.

11.17 Resets

There are several kinds of reset in the system.

Register Name	HPR
ADDR	$3F
bit 31	LCB_S(15)
bit 30	LCB_S(14)
bit 29	LCB_S(13)
bit 28	LCB_S(12)
bit 27	LCB_S(11)
bit 26	LCB_S(10)
bit 25	LCB_S(9)
bit 24	LCB_S(8)
bit 23	LCB_S(7)
bit 22	LCB_S(6)
bit 21	LCB_S(5)
bit 20	LCB_S(4)
bit 19	LCB_S(3)
bit 18	LCB_S(2)
bit 17	LCB_S(1)
bit 16	LCB_S(0)
bit 15	LCB_SCmd_Err
bit 14	LCB_ErrCnt_Ovfl
bit 13	LCB_Decode_Err
bit 12	LCB_Locked
bit 11	ADC_dat(11)
bit 10	ADC_dat(10)
bit 9	ADC_dat(9)
bit 8	ADC_dat(8)
bit 7	ADC_dat(7)
bit 6	ADC_dat(6)
bit 5	ADC_dat(5)
bit 4	ADC_dat(4)
bit 3	ADC_dat(3)
bit 2	ADC_dat(2)
bit 1	ADC_dat(1)
bit 0	ADC_dat(0)
SEUbit	no
Reset Value (hex)	00000000

Table 11.41: HIGH PRIORITY REGISTER $3F

11.17.1 RSTB pin

The external reset pin acts as a general asynchronous reset, identical to Power up Reset in term of action on the chip.

11.17.2 Power up Reset

The power-up reset is an asynchronous (i.e. clock independent) reset that sets the value of the chips registers to their default value, and clears all FIFOS in the chip (but not the L0Buffer nor EvtBuffer), thus placing the chip into a well defined state. This type of reset is issued automatically when power is applied to the chip. It can be supplied externally to the chip, through the input RSTB_pad.

11.17.3 Register_Reset (RegReset)

This type of reset is sent to the chip via a command instruction. Its purpose is to reset all the registers to their default value, and clears the pointers and readout mechanism, hence losing the chip configuration and the physics data. It should result in a chip being in the same status as after a power-up reset.

11.17.4 Logic_Reset (LogReset)

This type of reset is sent to the chip via a command instruction. Its purpose is to clear all the state machines and FIFOs in the chip, while leaving the configuration of the chip unaffected. This type of reset can be issued to the chip periodically during data taking to eliminate synchronization errors.

Note: Upon receipt of the Logic_Reset command, the ABCStar chip resets all internal counters and clears pending operations. If it was transmitting data, it terminates this immediately.

Register Name	TrimDAC0	TrimDAC1	TrimDAC2	TrimDAC3
ADDR	$40	$41	$42	$43
bit 31	TRIMDAC_CH7(3)	TRIMDAC_CH15(3)	TRIMDAC_CH23(3)	TRIMDAC_CH31(3)
bit 30	TRIMDAC_CH7(2)	TRIMDAC_CH15(2)	TRIMDAC_CH23(2)	TRIMDAC_CH31(2)
bit 29	TRIMDAC_CH7(1)	TRIMDAC_CH15(1)	TRIMDAC_CH23(1)	TRIMDAC_CH31(1)
bit 28	TRIMDAC_CH7(0)	TRIMDAC_CH15(0)	TRIMDAC_CH23(0)	TRIMDAC_CH31(0)
bit 27	TRIMDAC_CH5(3)	TRIMDAC_CH13(3)	TRIMDAC_CH21(3)	TRIMDAC_CH29(3)
bit 26	TRIMDAC_CH5(2)	TRIMDAC_CH13(2)	TRIMDAC_CH21(2)	TRIMDAC_CH29(2)
bit 25	TRIMDAC_CH5(1)	TRIMDAC_CH13(1)	TRIMDAC_CH21(1)	TRIMDAC_CH29(1)
bit 24	TRIMDAC_CH5(0)	TRIMDAC_CH13(0)	TRIMDAC_CH21(0)	TRIMDAC_CH29(0)
bit 23	TRIMDAC_CH6(3)	TRIMDAC_CH14(3)	TRIMDAC_CH22(3)	TRIMDAC_CH30(3)
bit 22	TRIMDAC_CH6(2)	TRIMDAC_CH14(2)	TRIMDAC_CH22(2)	TRIMDAC_CH30(2)
bit 21	TRIMDAC_CH6(1)	TRIMDAC_CH14(1)	TRIMDAC_CH22(1)	TRIMDAC_CH30(1)
bit 20	TRIMDAC_CH6(0)	TRIMDAC_CH14(0)	TRIMDAC_CH22(0)	TRIMDAC_CH30(0)
bit 19	TRIMDAC_CH4(3)	TRIMDAC_CH12(3)	TRIMDAC_CH20(3)	TRIMDAC_CH28(3)
bit 18	TRIMDAC_CH4(2)	TRIMDAC_CH12(2)	TRIMDAC_CH20(2)	TRIMDAC_CH28(2)
bit 17	TRIMDAC_CH4(1)	TRIMDAC_CH12(1)	TRIMDAC_CH20(1)	TRIMDAC_CH28(1)
bit 16	TRIMDAC_CH4(0)	TRIMDAC_CH12(0)	TRIMDAC_CH20(0)	TRIMDAC_CH28(0)
bit 15	TRIMDAC_CH3(3)	TRIMDAC_CH11(3)	TRIMDAC_CH19(3)	TRIMDAC_CH27(3)
bit 14	TRIMDAC_CH3(2)	TRIMDAC_CH11(2)	TRIMDAC_CH19(2)	TRIMDAC_CH27(2)
bit 13	TRIMDAC_CH3(1)	TRIMDAC_CH11(1)	TRIMDAC_CH19(1)	TRIMDAC_CH27(1)
bit 12	TRIMDAC_CH3(0)	TRIMDAC_CH11(0)	TRIMDAC_CH19(0)	TRIMDAC_CH27(0)
bit 11	TRIMDAC_CH1(3)	TRIMDAC_CH9(3)	TRIMDAC_CH17(3)	TRIMDAC_CH25(3)
bit 10	TRIMDAC_CH1(2)	TRIMDAC_CH9(2)	TRIMDAC_CH17(2)	TRIMDAC_CH25(2)
bit 9	TRIMDAC_CH1(1)	TRIMDAC_CH9(1)	TRIMDAC_CH17(1)	TRIMDAC_CH25(1)
bit 8	TRIMDAC_CH1(0)	TRIMDAC_CH9(0)	TRIMDAC_CH17(0)	TRIMDAC_CH25(0)
bit 7	TRIMDAC_CH2(3)	TRIMDAC_CH10(3)	TRIMDAC_CH18(3)	TRIMDAC_CH26(3)
bit 6	TRIMDAC_CH2(2)	TRIMDAC_CH10(2)	TRIMDAC_CH18(2)	TRIMDAC_CH26(2)
bit 5	TRIMDAC_CH2(1)	TRIMDAC_CH10(1)	TRIMDAC_CH18(1)	TRIMDAC_CH26(1)
bit 4	TRIMDAC_CH2(0)	TRIMDAC_CH10(0)	TRIMDAC_CH18(0)	TRIMDAC_CH26(0)
bit 3	TRIMDAC_CH0(3)	TRIMDAC_CH8(3)	TRIMDAC_CH16(3)	TRIMDAC_CH24(3)
bit 2	TRIMDAC_CH0(2)	TRIMDAC_CH8(2)	TRIMDAC_CH16(2)	TRIMDAC_CH24(2)
bit 1	TRIMDAC_CH0(1)	TRIMDAC_CH8(1)	TRIMDAC_CH16(1)	TRIMDAC_CH24(1)
bit 0	TRIMDAC_CH0(0)	TRIMDAC_CH8(0)	TRIMDAC_CH16(0)	TRIMDAC_CH24(0)
SEUbit	CR3SEU	CR3SEU	CR3SEU	CR3SEU
Reset Value (hex)	00000000	00000000	00000000	00000000

Table 11.42: TrimDAC registers (0 to 3)

11.17.5 SEU Reset

This type of reset is sent to the chip via a command instruction. Its purpose is to reset the bits tagging SEU events in the register $30.

11.17.6 BC Reset (BCR)

This type of reset is sent to the chip via a fast command. Its purpose is to zero the Beam Crossing counter. It has no effect on the operation of any other part of the chip.

11.17.7 Slow Command Reset

This type of reset is sent to the chip via a fast command. Its purpose is to reset the state machine in the LCB circuit which handles slow commands (more precisely, the RegBlock Interface state machine).

11.18 Default Register Values

On power up, RST_b low to high, or Register_Reset command, the contents of the configuration registers will be set to default. This results in the following configuration (summary) :

- Minimum Bias currents for the analogue channels
- Maximum channel threshold value
- TrimDACS setting at 0
- All calibration enable at 0

Register Name	TrimDAC4	TrimDAC5	TrimDAC6	TrimDAC7
ADDR	$44	$45	$46	$47
bit 31	TRIMDAC_CH39(3)	TRIMDAC_CH47(3)	TRIMDAC_CH55(3)	TRIMDAC_CH63(3)
bit 30	TRIMDAC_CH39(2)	TRIMDAC_CH47(2)	TRIMDAC_CH55(2)	TRIMDAC_CH63(2)
bit 29	TRIMDAC_CH39(1)	TRIMDAC_CH47(1)	TRIMDAC_CH55(1)	TRIMDAC_CH63(1)
bit 28	TRIMDAC_CH39(0)	TRIMDAC_CH47(0)	TRIMDAC_CH55(0)	TRIMDAC_CH63(0)
bit 27	TRIMDAC_CH37(3)	TRIMDAC_CH45(3)	TRIMDAC_CH53(3)	TRIMDAC_CH61(3)
bit 26	TRIMDAC_CH37(2)	TRIMDAC_CH45(2)	TRIMDAC_CH53(2)	TRIMDAC_CH61(2)
bit 25	TRIMDAC_CH37(1)	TRIMDAC_CH45(1)	TRIMDAC_CH53(1)	TRIMDAC_CH61(1)
bit 24	TRIMDAC_CH37(0)	TRIMDAC_CH45(0)	TRIMDAC_CH53(0)	TRIMDAC_CH61(0)
bit 23	TRIMDAC_CH38(3)	TRIMDAC_CH46(3)	TRIMDAC_CH54(3)	TRIMDAC_CH62(3)
bit 22	TRIMDAC_CH38(2)	TRIMDAC_CH46(2)	TRIMDAC_CH54(2)	TRIMDAC_CH62(2)
bit 21	TRIMDAC_CH38(1)	TRIMDAC_CH46(1)	TRIMDAC_CH54(1)	TRIMDAC_CH62(1)
bit 20	TRIMDAC_CH38(0)	TRIMDAC_CH46(0)	TRIMDAC_CH54(0)	TRIMDAC_CH62(0)
bit 19	TRIMDAC_CH36(3)	TRIMDAC_CH44(3)	TRIMDAC_CH52(3)	TRIMDAC_CH60(3)
bit 18	TRIMDAC_CH36(2)	TRIMDAC_CH44(2)	TRIMDAC_CH52(2)	TRIMDAC_CH60(2)
bit 17	TRIMDAC_CH36(1)	TRIMDAC_CH44(1)	TRIMDAC_CH52(1)	TRIMDAC_CH60(1)
bit 16	TRIMDAC_CH36(0)	TRIMDAC_CH44(0)	TRIMDAC_CH52(0)	TRIMDAC_CH60(0)
bit 15	TRIMDAC_CH35(3)	TRIMDAC_CH43(3)	TRIMDAC_CH51(3)	TRIMDAC_CH59(3)
bit 14	TRIMDAC_CH35(2)	TRIMDAC_CH43(2)	TRIMDAC_CH51(2)	TRIMDAC_CH59(2)
bit 13	TRIMDAC_CH35(1)	TRIMDAC_CH43(1)	TRIMDAC_CH51(1)	TRIMDAC_CH59(1)
bit 12	TRIMDAC_CH35(0)	TRIMDAC_CH43(0)	TRIMDAC_CH51(0)	TRIMDAC_CH59(0)
bit 11	TRIMDAC_CH33(3)	TRIMDAC_CH41(3)	TRIMDAC_CH49(3)	TRIMDAC_CH57(3)
bit 10	TRIMDAC_CH33(2)	TRIMDAC_CH41(2)	TRIMDAC_CH49(2)	TRIMDAC_CH57(2)
bit 9	TRIMDAC_CH33(1)	TRIMDAC_CH41(1)	TRIMDAC_CH49(1)	TRIMDAC_CH57(1)
bit 8	TRIMDAC_CH33(0)	TRIMDAC_CH41(0)	TRIMDAC_CH49(0)	TRIMDAC_CH57(0)
bit 7	TRIMDAC_CH34(3)	TRIMDAC_CH42(3)	TRIMDAC_CH50(3)	TRIMDAC_CH58(3)
bit 6	TRIMDAC_CH34(2)	TRIMDAC_CH42(2)	TRIMDAC_CH50(2)	TRIMDAC_CH58(2)
bit 5	TRIMDAC_CH34(1)	TRIMDAC_CH42(1)	TRIMDAC_CH50(1)	TRIMDAC_CH58(1)
bit 4	TRIMDAC_CH34(0)	TRIMDAC_CH42(0)	TRIMDAC_CH50(0)	TRIMDAC_CH58(0)
bit 3	TRIMDAC_CH32(3)	TRIMDAC_CH40(3)	TRIMDAC_CH48(3)	TRIMDAC_CH56(3)
bit 2	TRIMDAC_CH32(2)	TRIMDAC_CH40(2)	TRIMDAC_CH48(2)	TRIMDAC_CH56(2)
bit 1	TRIMDAC_CH32(1)	TRIMDAC_CH40(1)	TRIMDAC_CH48(1)	TRIMDAC_CH56(1)
bit 0	TRIMDAC_CH32(0)	TRIMDAC_CH40(0)	TRIMDAC_CH48(0)	TRIMDAC_CH56(0)
SEUbit	CR7SEU	CR7SEU	CR7SEU	CR7SEU
Reset Value (hex)	00000000	00000000	00000000	00000000

Table 11.43: TrimDAC registers (4 to 7)

Register Name	TrimDAC8	TrimDAC9	TrimDAC10	TrimDAC11
ADDR	$48	$49	$4a	$4b
bit 31	TRIMDAC_CH71(3)	TRIMDAC_CH79(3)	TRIMDAC_CH87(3)	TRIMDAC_CH95(3)
bit 30	TRIMDAC_CH71(2)	TRIMDAC_CH79(2)	TRIMDAC_CH87(2)	TRIMDAC_CH95(2)
bit 29	TRIMDAC_CH71(1)	TRIMDAC_CH79(1)	TRIMDAC_CH87(1)	TRIMDAC_CH95(1)
bit 28	TRIMDAC_CH71(0)	TRIMDAC_CH79(0)	TRIMDAC_CH87(0)	TRIMDAC_CH95(0)
bit 27	TRIMDAC_CH69(3)	TRIMDAC_CH77(3)	TRIMDAC_CH85(3)	TRIMDAC_CH93(3)
bit 26	TRIMDAC_CH69(2)	TRIMDAC_CH77(2)	TRIMDAC_CH85(2)	TRIMDAC_CH93(2)
bit 25	TRIMDAC_CH69(1)	TRIMDAC_CH77(1)	TRIMDAC_CH85(1)	TRIMDAC_CH93(1)
bit 24	TRIMDAC_CH69(0)	TRIMDAC_CH77(0)	TRIMDAC_CH85(0)	TRIMDAC_CH93(0)
bit 23	TRIMDAC_CH70(3)	TRIMDAC_CH78(3)	TRIMDAC_CH86(3)	TRIMDAC_CH94(3)
bit 22	TRIMDAC_CH70(2)	TRIMDAC_CH78(2)	TRIMDAC_CH86(2)	TRIMDAC_CH94(2)
bit 21	TRIMDAC_CH70(1)	TRIMDAC_CH78(1)	TRIMDAC_CH86(1)	TRIMDAC_CH94(1)
bit 20	TRIMDAC_CH70(0)	TRIMDAC_CH78(0)	TRIMDAC_CH86(0)	TRIMDAC_CH94(0)
bit 19	TRIMDAC_CH68(3)	TRIMDAC_CH76(3)	TRIMDAC_CH84(3)	TRIMDAC_CH92(3)
bit 18	TRIMDAC_CH68(2)	TRIMDAC_CH76(2)	TRIMDAC_CH84(2)	TRIMDAC_CH92(2)
bit 17	TRIMDAC_CH68(1)	TRIMDAC_CH76(1)	TRIMDAC_CH84(1)	TRIMDAC_CH92(1)
bit 16	TRIMDAC_CH68(0)	TRIMDAC_CH76(0)	TRIMDAC_CH84(0)	TRIMDAC_CH92(0)
bit 15	TRIMDAC_CH67(3)	TRIMDAC_CH75(3)	TRIMDAC_CH83(3)	TRIMDAC_CH91(3)
bit 14	TRIMDAC_CH67(2)	TRIMDAC_CH75(2)	TRIMDAC_CH83(2)	TRIMDAC_CH91(2)
bit 13	TRIMDAC_CH67(1)	TRIMDAC_CH75(1)	TRIMDAC_CH83(1)	TRIMDAC_CH91(1)
bit 12	TRIMDAC_CH67(0)	TRIMDAC_CH75(0)	TRIMDAC_CH83(0)	TRIMDAC_CH91(0)
bit 11	TRIMDAC_CH65(3)	TRIMDAC_CH73(3)	TRIMDAC_CH81(3)	TRIMDAC_CH89(3)
bit 10	TRIMDAC_CH65(2)	TRIMDAC_CH73(2)	TRIMDAC_CH81(2)	TRIMDAC_CH89(2)
bit 9	TRIMDAC_CH65(1)	TRIMDAC_CH73(1)	TRIMDAC_CH81(1)	TRIMDAC_CH89(1)
bit 8	TRIMDAC_CH65(0)	TRIMDAC_CH73(0)	TRIMDAC_CH81(0)	TRIMDAC_CH89(0)
bit 7	TRIMDAC_CH66(3)	TRIMDAC_CH74(3)	TRIMDAC_CH82(3)	TRIMDAC_CH90(3)
bit 6	TRIMDAC_CH66(2)	TRIMDAC_CH74(2)	TRIMDAC_CH82(2)	TRIMDAC_CH90(2)
bit 5	TRIMDAC_CH66(1)	TRIMDAC_CH74(1)	TRIMDAC_CH82(1)	TRIMDAC_CH90(1)
bit 4	TRIMDAC_CH66(0)	TRIMDAC_CH74(0)	TRIMDAC_CH82(0)	TRIMDAC_CH90(0)
bit 3	TRIMDAC_CH64(3)	TRIMDAC_CH72(3)	TRIMDAC_CH80(3)	TRIMDAC_CH88(3)
bit 2	TRIMDAC_CH64(2)	TRIMDAC_CH72(2)	TRIMDAC_CH80(2)	TRIMDAC_CH88(2)
bit 1	TRIMDAC_CH64(1)	TRIMDAC_CH72(1)	TRIMDAC_CH80(1)	TRIMDAC_CH88(1)
bit 0	TRIMDAC_CH64(0)	TRIMDAC_CH72(0)	TRIMDAC_CH80(0)	TRIMDAC_CH88(0)
SEUbit	CR11SEU	CR11SEU	CR11SEU	CR11SEU
Reset Value (hex)	00000000	00000000	00000000	00000000

Table 11.44: TrimDAC registers (8 to 11)

Register Name	TrimDAC12	TrimDAC13	TrimDAC14	TrimDAC15
ADDR	$4c	$4d	$4e	$4f
bit 31	TRIMDAC_CH103(3)	TRIMDAC_CH111(3)	TRIMDAC_CH119(3)	TRIMDAC_CH127(3)
bit 30	TRIMDAC_CH103(2)	TRIMDAC_CH111(2)	TRIMDAC_CH119(2)	TRIMDAC_CH127(2)
bit 29	TRIMDAC_CH103(1)	TRIMDAC_CH111(1)	TRIMDAC_CH119(1)	TRIMDAC_CH127(1)
bit 28	TRIMDAC_CH103(0)	TRIMDAC_CH111(0)	TRIMDAC_CH119(0)	TRIMDAC_CH127(0)
bit 27	TRIMDAC_CH101(3)	TRIMDAC_CH109(3)	TRIMDAC_CH117(3)	TRIMDAC_CH125(3)
bit 26	TRIMDAC_CH101(2)	TRIMDAC_CH109(2)	TRIMDAC_CH117(2)	TRIMDAC_CH125(2)
bit 25	TRIMDAC_CH101(1)	TRIMDAC_CH109(1)	TRIMDAC_CH117(1)	TRIMDAC_CH125(1)
bit 24	TRIMDAC_CH101(0)	TRIMDAC_CH109(0)	TRIMDAC_CH117(0)	TRIMDAC_CH125(0)
bit 23	TRIMDAC_CH102(3)	TRIMDAC_CH110(3)	TRIMDAC_CH118(3)	TRIMDAC_CH126(3)
bit 22	TRIMDAC_CH102(2)	TRIMDAC_CH110(2)	TRIMDAC_CH118(2)	TRIMDAC_CH126(2)
bit 21	TRIMDAC_CH102(1)	TRIMDAC_CH110(1)	TRIMDAC_CH118(1)	TRIMDAC_CH126(1)
bit 20	TRIMDAC_CH102(0)	TRIMDAC_CH110(0)	TRIMDAC_CH118(0)	TRIMDAC_CH126(0)
bit 19	TRIMDAC_CH100(3)	TRIMDAC_CH108(3)	TRIMDAC_CH116(3)	TRIMDAC_CH124(3)
bit 18	TRIMDAC_CH100(2)	TRIMDAC_CH108(2)	TRIMDAC_CH116(2)	TRIMDAC_CH124(2)
bit 17	TRIMDAC_CH100(1)	TRIMDAC_CH108(1)	TRIMDAC_CH116(1)	TRIMDAC_CH124(1)
bit 16	TRIMDAC_CH100(0)	TRIMDAC_CH108(0)	TRIMDAC_CH116(0)	TRIMDAC_CH124(0)
bit 15	TRIMDAC_CH99(3)	TRIMDAC_CH107(3)	TRIMDAC_CH115(3)	TRIMDAC_CH123(3)
bit 14	TRIMDAC_CH99(2)	TRIMDAC_CH107(2)	TRIMDAC_CH115(2)	TRIMDAC_CH123(2)
bit 13	TRIMDAC_CH99(1)	TRIMDAC_CH107(1)	TRIMDAC_CH115(1)	TRIMDAC_CH123(1)
bit 12	TRIMDAC_CH99(0)	TRIMDAC_CH107(0)	TRIMDAC_CH115(0)	TRIMDAC_CH123(0)
bit 11	TRIMDAC_CH97(3)	TRIMDAC_CH105(3)	TRIMDAC_CH113(3)	TRIMDAC_CH121(3)
bit 10	TRIMDAC_CH97(2)	TRIMDAC_CH105(2)	TRIMDAC_CH113(2)	TRIMDAC_CH121(2)
bit 9	TRIMDAC_CH97(1)	TRIMDAC_CH105(1)	TRIMDAC_CH113(1)	TRIMDAC_CH121(1)
bit 8	TRIMDAC_CH97(0)	TRIMDAC_CH105(0)	TRIMDAC_CH113(0)	TRIMDAC_CH121(0)
bit 7	TRIMDAC_CH98(3)	TRIMDAC_CH106(3)	TRIMDAC_CH114(3)	TRIMDAC_CH122(3)
bit 6	TRIMDAC_CH98(2)	TRIMDAC_CH106(2)	TRIMDAC_CH114(2)	TRIMDAC_CH122(2)
bit 5	TRIMDAC_CH98(1)	TRIMDAC_CH106(1)	TRIMDAC_CH114(1)	TRIMDAC_CH122(1)
bit 4	TRIMDAC_CH98(0)	TRIMDAC_CH106(0)	TRIMDAC_CH114(0)	TRIMDAC_CH122(0)
bit 3	TRIMDAC_CH96(3)	TRIMDAC_CH104(3)	TRIMDAC_CH112(3)	TRIMDAC_CH120(3)
bit 2	TRIMDAC_CH96(2)	TRIMDAC_CH104(2)	TRIMDAC_CH112(2)	TRIMDAC_CH120(2)
bit 1	TRIMDAC_CH96(1)	TRIMDAC_CH104(1)	TRIMDAC_CH112(1)	TRIMDAC_CH120(1)
bit 0	TRIMDAC_CH96(0)	TRIMDAC_CH104(0)	TRIMDAC_CH112(0)	TRIMDAC_CH120(0)
SEUbit	CR15SEU	CR15SEU	CR15SEU	CR15SEU
Reset Value (hex)	00000000	00000000	00000000	00000000

Table 11.45: TrimDAC registers (12 to 15)

Register Name	TrimDAC16	TrimDAC17	TrimDAC18	TrimDAC19
ADDR	$50	$51	$52	$53
bit 31	TRIMDAC_CH135(3)	TRIMDAC_CH143(3)	TRIMDAC_CH151(3)	TRIMDAC_CH159(3)
bit 30	TRIMDAC_CH135(2)	TRIMDAC_CH143(2)	TRIMDAC_CH151(2)	TRIMDAC_CH159(2)
bit 29	TRIMDAC_CH135(1)	TRIMDAC_CH143(1)	TRIMDAC_CH151(1)	TRIMDAC_CH159(1)
bit 28	TRIMDAC_CH135(0)	TRIMDAC_CH143(0)	TRIMDAC_CH151(0)	TRIMDAC_CH159(0)
bit 27	TRIMDAC_CH133(3)	TRIMDAC_CH141(3)	TRIMDAC_CH149(3)	TRIMDAC_CH157(3)
bit 26	TRIMDAC_CH133(2)	TRIMDAC_CH141(2)	TRIMDAC_CH149(2)	TRIMDAC_CH157(2)
bit 25	TRIMDAC_CH133(1)	TRIMDAC_CH141(1)	TRIMDAC_CH149(1)	TRIMDAC_CH157(1)
bit 24	TRIMDAC_CH133(0)	TRIMDAC_CH141(0)	TRIMDAC_CH149(0)	TRIMDAC_CH157(0)
bit 23	TRIMDAC_CH134(3)	TRIMDAC_CH142(3)	TRIMDAC_CH150(3)	TRIMDAC_CH158(3)
bit 22	TRIMDAC_CH134(2)	TRIMDAC_CH142(2)	TRIMDAC_CH150(2)	TRIMDAC_CH158(2)
bit 21	TRIMDAC_CH134(1)	TRIMDAC_CH142(1)	TRIMDAC_CH150(1)	TRIMDAC_CH158(1)
bit 20	TRIMDAC_CH134(0)	TRIMDAC_CH142(0)	TRIMDAC_CH150(0)	TRIMDAC_CH158(0)
bit 19	TRIMDAC_CH132(3)	TRIMDAC_CH140(3)	TRIMDAC_CH148(3)	TRIMDAC_CH156(3)
bit 18	TRIMDAC_CH132(2)	TRIMDAC_CH140(2)	TRIMDAC_CH148(2)	TRIMDAC_CH156(2)
bit 17	TRIMDAC_CH132(1)	TRIMDAC_CH140(1)	TRIMDAC_CH148(1)	TRIMDAC_CH156(1)
bit 16	TRIMDAC_CH132(0)	TRIMDAC_CH140(0)	TRIMDAC_CH148(0)	TRIMDAC_CH156(0)
bit 15	TRIMDAC_CH131(3)	TRIMDAC_CH139(3)	TRIMDAC_CH147(3)	TRIMDAC_CH155(3)
bit 14	TRIMDAC_CH131(2)	TRIMDAC_CH139(2)	TRIMDAC_CH147(2)	TRIMDAC_CH155(2)
bit 13	TRIMDAC_CH131(1)	TRIMDAC_CH139(1)	TRIMDAC_CH147(1)	TRIMDAC_CH155(1)
bit 12	TRIMDAC_CH131(0)	TRIMDAC_CH139(0)	TRIMDAC_CH147(0)	TRIMDAC_CH155(0)
bit 11	TRIMDAC_CH129(3)	TRIMDAC_CH137(3)	TRIMDAC_CH145(3)	TRIMDAC_CH153(3)
bit 10	TRIMDAC_CH129(2)	TRIMDAC_CH137(2)	TRIMDAC_CH145(2)	TRIMDAC_CH153(2)
bit 9	TRIMDAC_CH129(1)	TRIMDAC_CH137(1)	TRIMDAC_CH145(1)	TRIMDAC_CH153(1)
bit 8	TRIMDAC_CH129(0)	TRIMDAC_CH137(0)	TRIMDAC_CH145(0)	TRIMDAC_CH153(0)
bit 7	TRIMDAC_CH130(3)	TRIMDAC_CH138(3)	TRIMDAC_CH146(3)	TRIMDAC_CH154(3)
bit 6	TRIMDAC_CH130(2)	TRIMDAC_CH138(2)	TRIMDAC_CH146(2)	TRIMDAC_CH154(2)
bit 5	TRIMDAC_CH130(1)	TRIMDAC_CH138(1)	TRIMDAC_CH146(1)	TRIMDAC_CH154(1)
bit 4	TRIMDAC_CH130(0)	TRIMDAC_CH138(0)	TRIMDAC_CH146(0)	TRIMDAC_CH154(0)
bit 3	TRIMDAC_CH128(3)	TRIMDAC_CH136(3)	TRIMDAC_CH144(3)	TRIMDAC_CH152(3)
bit 2	TRIMDAC_CH128(2)	TRIMDAC_CH136(2)	TRIMDAC_CH144(2)	TRIMDAC_CH152(2)
bit 1	TRIMDAC_CH128(1)	TRIMDAC_CH136(1)	TRIMDAC_CH144(1)	TRIMDAC_CH152(1)
bit 0	TRIMDAC_CH128(0)	TRIMDAC_CH136(0)	TRIMDAC_CH144(0)	TRIMDAC_CH152(0)
SEUbit	CR19SEU	CR19SEU	CR19SEU	CR19SEU
Reset Value (hex)	00000000	00000000	00000000	00000000

Table 11.46: TrimDAC registers (16 to 19)

Register Name	TrimDAC20	TrimDAC21	TrimDAC22	TrimDAC23
ADDR	$54	$55	$56	$57
bit 31	TRIMDAC_CH167(3)	TRIMDAC_CH175(3)	TRIMDAC_CH183(3)	TRIMDAC_CH191(3)
bit 30	TRIMDAC_CH167(2)	TRIMDAC_CH175(2)	TRIMDAC_CH183(2)	TRIMDAC_CH191(2)
bit 29	TRIMDAC_CH167(1)	TRIMDAC_CH175(1)	TRIMDAC_CH183(1)	TRIMDAC_CH191(1)
bit 28	TRIMDAC_CH167(0)	TRIMDAC_CH175(0)	TRIMDAC_CH183(0)	TRIMDAC_CH191(0)
bit 27	TRIMDAC_CH165(3)	TRIMDAC_CH173(3)	TRIMDAC_CH181(3)	TRIMDAC_CH189(3)
bit 26	TRIMDAC_CH165(2)	TRIMDAC_CH173(2)	TRIMDAC_CH181(2)	TRIMDAC_CH189(2)
bit 25	TRIMDAC_CH165(1)	TRIMDAC_CH173(1)	TRIMDAC_CH181(1)	TRIMDAC_CH189(1)
bit 24	TRIMDAC_CH165(0)	TRIMDAC_CH173(0)	TRIMDAC_CH181(0)	TRIMDAC_CH189(0)
bit 23	TRIMDAC_CH166(3)	TRIMDAC_CH174(3)	TRIMDAC_CH182(3)	TRIMDAC_CH190(3)
bit 22	TRIMDAC_CH166(2)	TRIMDAC_CH174(2)	TRIMDAC_CH182(2)	TRIMDAC_CH190(2)
bit 21	TRIMDAC_CH166(1)	TRIMDAC_CH174(1)	TRIMDAC_CH182(1)	TRIMDAC_CH190(1)
bit 20	TRIMDAC_CH166(0)	TRIMDAC_CH174(0)	TRIMDAC_CH182(0)	TRIMDAC_CH190(0)
bit 19	TRIMDAC_CH164(3)	TRIMDAC_CH172(3)	TRIMDAC_CH180(3)	TRIMDAC_CH188(3)
bit 18	TRIMDAC_CH164(2)	TRIMDAC_CH172(2)	TRIMDAC_CH180(2)	TRIMDAC_CH188(2)
bit 17	TRIMDAC_CH164(1)	TRIMDAC_CH172(1)	TRIMDAC_CH180(1)	TRIMDAC_CH188(1)
bit 16	TRIMDAC_CH164(0)	TRIMDAC_CH172(0)	TRIMDAC_CH180(0)	TRIMDAC_CH188(0)
bit 15	TRIMDAC_CH163(3)	TRIMDAC_CH171(3)	TRIMDAC_CH179(3)	TRIMDAC_CH187(3)
bit 14	TRIMDAC_CH163(2)	TRIMDAC_CH171(2)	TRIMDAC_CH179(2)	TRIMDAC_CH187(2)
bit 13	TRIMDAC_CH163(1)	TRIMDAC_CH171(1)	TRIMDAC_CH179(1)	TRIMDAC_CH187(1)
bit 12	TRIMDAC_CH163(0)	TRIMDAC_CH171(0)	TRIMDAC_CH179(0)	TRIMDAC_CH187(0)
bit 11	TRIMDAC_CH161(3)	TRIMDAC_CH169(3)	TRIMDAC_CH177(3)	TRIMDAC_CH185(3)
bit 10	TRIMDAC_CH161(2)	TRIMDAC_CH169(2)	TRIMDAC_CH177(2)	TRIMDAC_CH185(2)
bit 9	TRIMDAC_CH161(1)	TRIMDAC_CH169(1)	TRIMDAC_CH177(1)	TRIMDAC_CH185(1)
bit 8	TRIMDAC_CH161(0)	TRIMDAC_CH169(0)	TRIMDAC_CH177(0)	TRIMDAC_CH185(0)
bit 7	TRIMDAC_CH162(3)	TRIMDAC_CH170(3)	TRIMDAC_CH178(3)	TRIMDAC_CH186(3)
bit 6	TRIMDAC_CH162(2)	TRIMDAC_CH170(2)	TRIMDAC_CH178(2)	TRIMDAC_CH186(2)
bit 5	TRIMDAC_CH162(1)	TRIMDAC_CH170(1)	TRIMDAC_CH178(1)	TRIMDAC_CH186(1)
bit 4	TRIMDAC_CH162(0)	TRIMDAC_CH170(0)	TRIMDAC_CH178(0)	TRIMDAC_CH186(0)
bit 3	TRIMDAC_CH160(3)	TRIMDAC_CH168(3)	TRIMDAC_CH176(3)	TRIMDAC_CH184(3)
bit 2	TRIMDAC_CH160(2)	TRIMDAC_CH168(2)	TRIMDAC_CH176(2)	TRIMDAC_CH184(2)
bit 1	TRIMDAC_CH160(1)	TRIMDAC_CH168(1)	TRIMDAC_CH176(1)	TRIMDAC_CH184(1)
bit 0	TRIMDAC_CH160(0)	TRIMDAC_CH168(0)	TRIMDAC_CH176(0)	TRIMDAC_CH184(0)
SEUbit	CR23SEU	CR23SEU	CR23SEU	CR23SEU
Reset Value (hex)	00000000	00000000	00000000	00000000

Table 11.47: TrimDAC registers (20 to 23)

Register Name	TrimDAC24	TrimDAC25	TrimDAC26	TrimDAC27
ADDR	$58	$59	$5a	$5b
bit 31	TRIMDAC_CH199(3)	TRIMDAC_CH207(3)	TRIMDAC_CH215(3)	TRIMDAC_CH223(3)
bit 30	TRIMDAC_CH199(2)	TRIMDAC_CH207(2)	TRIMDAC_CH215(2)	TRIMDAC_CH223(2)
bit 29	TRIMDAC_CH199(1)	TRIMDAC_CH207(1)	TRIMDAC_CH215(1)	TRIMDAC_CH223(1)
bit 28	TRIMDAC_CH199(0)	TRIMDAC_CH207(0)	TRIMDAC_CH215(0)	TRIMDAC_CH223(0)
bit 27	TRIMDAC_CH197(3)	TRIMDAC_CH205(3)	TRIMDAC_CH213(3)	TRIMDAC_CH221(3)
bit 26	TRIMDAC_CH197(2)	TRIMDAC_CH205(2)	TRIMDAC_CH213(2)	TRIMDAC_CH221(2)
bit 25	TRIMDAC_CH197(1)	TRIMDAC_CH205(1)	TRIMDAC_CH213(1)	TRIMDAC_CH221(1)
bit 24	TRIMDAC_CH197(0)	TRIMDAC_CH205(0)	TRIMDAC_CH213(0)	TRIMDAC_CH221(0)
bit 23	TRIMDAC_CH198(3)	TRIMDAC_CH206(3)	TRIMDAC_CH214(3)	TRIMDAC_CH222(3)
bit 22	TRIMDAC_CH198(2)	TRIMDAC_CH206(2)	TRIMDAC_CH214(2)	TRIMDAC_CH222(2)
bit 21	TRIMDAC_CH198(1)	TRIMDAC_CH206(1)	TRIMDAC_CH214(1)	TRIMDAC_CH222(1)
bit 20	TRIMDAC_CH198(0)	TRIMDAC_CH206(0)	TRIMDAC_CH214(0)	TRIMDAC_CH222(0)
bit 19	TRIMDAC_CH196(3)	TRIMDAC_CH204(3)	TRIMDAC_CH212(3)	TRIMDAC_CH220(3)
bit 18	TRIMDAC_CH196(2)	TRIMDAC_CH204(2)	TRIMDAC_CH212(2)	TRIMDAC_CH220(2)
bit 17	TRIMDAC_CH196(1)	TRIMDAC_CH204(1)	TRIMDAC_CH212(1)	TRIMDAC_CH220(1)
bit 16	TRIMDAC_CH196(0)	TRIMDAC_CH204(0)	TRIMDAC_CH212(0)	TRIMDAC_CH220(0)
bit 15	TRIMDAC_CH195(3)	TRIMDAC_CH203(3)	TRIMDAC_CH211(3)	TRIMDAC_CH219(3)
bit 14	TRIMDAC_CH195(2)	TRIMDAC_CH203(2)	TRIMDAC_CH211(2)	TRIMDAC_CH219(2)
bit 13	TRIMDAC_CH195(1)	TRIMDAC_CH203(1)	TRIMDAC_CH211(1)	TRIMDAC_CH219(1)
bit 12	TRIMDAC_CH195(0)	TRIMDAC_CH203(0)	TRIMDAC_CH211(0)	TRIMDAC_CH219(0)
bit 11	TRIMDAC_CH193(3)	TRIMDAC_CH201(3)	TRIMDAC_CH209(3)	TRIMDAC_CH217(3)
bit 10	TRIMDAC_CH193(2)	TRIMDAC_CH201(2)	TRIMDAC_CH209(2)	TRIMDAC_CH217(2)
bit 9	TRIMDAC_CH193(1)	TRIMDAC_CH201(1)	TRIMDAC_CH209(1)	TRIMDAC_CH217(1)
bit 8	TRIMDAC_CH193(0)	TRIMDAC_CH201(0)	TRIMDAC_CH209(0)	TRIMDAC_CH217(0)
bit 7	TRIMDAC_CH194(3)	TRIMDAC_CH202(3)	TRIMDAC_CH210(3)	TRIMDAC_CH218(3)
bit 6	TRIMDAC_CH194(2)	TRIMDAC_CH202(2)	TRIMDAC_CH210(2)	TRIMDAC_CH218(2)
bit 5	TRIMDAC_CH194(1)	TRIMDAC_CH202(1)	TRIMDAC_CH210(1)	TRIMDAC_CH218(1)
bit 4	TRIMDAC_CH194(0)	TRIMDAC_CH202(0)	TRIMDAC_CH210(0)	TRIMDAC_CH218(0)
bit 3	TRIMDAC_CH192(3)	TRIMDAC_CH200(3)	TRIMDAC_CH208(3)	TRIMDAC_CH216(3)
bit 2	TRIMDAC_CH192(2)	TRIMDAC_CH200(2)	TRIMDAC_CH208(2)	TRIMDAC_CH216(2)
bit 1	TRIMDAC_CH192(1)	TRIMDAC_CH200(1)	TRIMDAC_CH208(1)	TRIMDAC_CH216(1)
bit 0	TRIMDAC_CH192(0)	TRIMDAC_CH200(0)	TRIMDAC_CH208(0)	TRIMDAC_CH216(0)
SEUbit	CR27SEU	CR27SEU	CR27SEU	CR27SEU
Reset Value (hex)	00000000	00000000	00000000	00000000

Table 11.48: TrimDAC registers (24 to 27)

Register Name	TrimDAC28	TrimDAC29	TrimDAC30	TrimDAC31
ADDR	$5c	$5d	$5e	$5f
bit 31	TRIMDAC_CH231(3)	TRIMDAC_CH239(3)	TRIMDAC_CH247(3)	TRIMDAC_CH255(3)
bit 30	TRIMDAC_CH231(2)	TRIMDAC_CH239(2)	TRIMDAC_CH247(2)	TRIMDAC_CH255(2)
bit 29	TRIMDAC_CH231(1)	TRIMDAC_CH239(1)	TRIMDAC_CH247(1)	TRIMDAC_CH255(1)
bit 28	TRIMDAC_CH231(0)	TRIMDAC_CH239(0)	TRIMDAC_CH247(0)	TRIMDAC_CH255(0)
bit 27	TRIMDAC_CH229(3)	TRIMDAC_CH237(3)	TRIMDAC_CH245(3)	TRIMDAC_CH253(3)
bit 26	TRIMDAC_CH229(2)	TRIMDAC_CH237(2)	TRIMDAC_CH245(2)	TRIMDAC_CH253(2)
bit 25	TRIMDAC_CH229(1)	TRIMDAC_CH237(1)	TRIMDAC_CH245(1)	TRIMDAC_CH253(1)
bit 24	TRIMDAC_CH229(0)	TRIMDAC_CH237(0)	TRIMDAC_CH245(0)	TRIMDAC_CH253(0)
bit 23	TRIMDAC_CH230(3)	TRIMDAC_CH238(3)	TRIMDAC_CH246(3)	TRIMDAC_CH254(3)
bit 22	TRIMDAC_CH230(2)	TRIMDAC_CH238(2)	TRIMDAC_CH246(2)	TRIMDAC_CH254(2)
bit 21	TRIMDAC_CH230(1)	TRIMDAC_CH238(1)	TRIMDAC_CH246(1)	TRIMDAC_CH254(1)
bit 20	TRIMDAC_CH230(0)	TRIMDAC_CH238(0)	TRIMDAC_CH246(0)	TRIMDAC_CH254(0)
bit 19	TRIMDAC_CH228(3)	TRIMDAC_CH236(3)	TRIMDAC_CH244(3)	TRIMDAC_CH252(3)
bit 18	TRIMDAC_CH228(2)	TRIMDAC_CH236(2)	TRIMDAC_CH244(2)	TRIMDAC_CH252(2)
bit 17	TRIMDAC_CH228(1)	TRIMDAC_CH236(1)	TRIMDAC_CH244(1)	TRIMDAC_CH252(1)
bit 16	TRIMDAC_CH228(0)	TRIMDAC_CH236(0)	TRIMDAC_CH244(0)	TRIMDAC_CH252(0)
bit 15	TRIMDAC_CH227(3)	TRIMDAC_CH235(3)	TRIMDAC_CH243(3)	TRIMDAC_CH251(3)
bit 14	TRIMDAC_CH227(2)	TRIMDAC_CH235(2)	TRIMDAC_CH243(2)	TRIMDAC_CH251(2)
bit 13	TRIMDAC_CH227(1)	TRIMDAC_CH235(1)	TRIMDAC_CH243(1)	TRIMDAC_CH251(1)
bit 12	TRIMDAC_CH227(0)	TRIMDAC_CH235(0)	TRIMDAC_CH243(0)	TRIMDAC_CH251(0)
bit 11	TRIMDAC_CH225(3)	TRIMDAC_CH233(3)	TRIMDAC_CH241(3)	TRIMDAC_CH249(3)
bit 10	TRIMDAC_CH225(2)	TRIMDAC_CH233(2)	TRIMDAC_CH241(2)	TRIMDAC_CH249(2)
bit 9	TRIMDAC_CH225(1)	TRIMDAC_CH233(1)	TRIMDAC_CH241(1)	TRIMDAC_CH249(1)
bit 8	TRIMDAC_CH225(0)	TRIMDAC_CH233(0)	TRIMDAC_CH241(0)	TRIMDAC_CH249(0)
bit 7	TRIMDAC_CH226(3)	TRIMDAC_CH234(3)	TRIMDAC_CH242(3)	TRIMDAC_CH250(3)
bit 6	TRIMDAC_CH226(2)	TRIMDAC_CH234(2)	TRIMDAC_CH242(2)	TRIMDAC_CH250(2)
bit 5	TRIMDAC_CH226(1)	TRIMDAC_CH234(1)	TRIMDAC_CH242(1)	TRIMDAC_CH250(1)
bit 4	TRIMDAC_CH226(0)	TRIMDAC_CH234(0)	TRIMDAC_CH242(0)	TRIMDAC_CH250(0)
bit 3	TRIMDAC_CH224(3)	TRIMDAC_CH232(3)	TRIMDAC_CH240(3)	TRIMDAC_CH248(3)
bit 2	TRIMDAC_CH224(2)	TRIMDAC_CH232(2)	TRIMDAC_CH240(2)	TRIMDAC_CH248(2)
bit 1	TRIMDAC_CH224(1)	TRIMDAC_CH232(1)	TRIMDAC_CH240(1)	TRIMDAC_CH248(1)
bit 0	TRIMDAC_CH224(0)	TRIMDAC_CH232(0)	TRIMDAC_CH240(0)	TRIMDAC_CH248(0)
SEUbit	CR31SEU	CR31SEU	CR31SEU	CR31SEU
Reset Value (hex)	00000000	00000000	00000000	00000000

Table 11.49: TrimDAC registers (28 to 31)

Register Name	TrimDAC32	TrimDAC33	TrimDAC34	TrimDAC35
ADDR	$60	$61	$62	$63
bit 31	TRIMDAC_CH31(4)	TRIMDAC_CH63(4)	TRIMDAC_CH95(4)	TRIMDAC_CH127(4)
bit 30	TRIMDAC_CH29(4)	TRIMDAC_CH61(4)	TRIMDAC_CH93(4)	TRIMDAC_CH125(4)
bit 29	TRIMDAC_CH30(4)	TRIMDAC_CH62(4)	TRIMDAC_CH94(4)	TRIMDAC_CH126(4)
bit 28	TRIMDAC_CH28(4)	TRIMDAC_CH60(4)	TRIMDAC_CH92(4)	TRIMDAC_CH124(4)
bit 27	TRIMDAC_CH27(4)	TRIMDAC_CH59(4)	TRIMDAC_CH91(4)	TRIMDAC_CH123(4)
bit 26	TRIMDAC_CH25(4)	TRIMDAC_CH57(4)	TRIMDAC_CH89(4)	TRIMDAC_CH121(4)
bit 25	TRIMDAC_CH26(4)	TRIMDAC_CH58(4)	TRIMDAC_CH90(4)	TRIMDAC_CH122(4)
bit 24	TRIMDAC_CH24(4)	TRIMDAC_CH56(4)	TRIMDAC_CH88(4)	TRIMDAC_CH120(4)
bit 23	TRIMDAC_CH23(4)	TRIMDAC_CH55(4)	TRIMDAC_CH87(4)	TRIMDAC_CH119(4)
bit 22	TRIMDAC_CH21(4)	TRIMDAC_CH53(4)	TRIMDAC_CH85(4)	TRIMDAC_CH117(4)
bit 21	TRIMDAC_CH22(4)	TRIMDAC_CH54(4)	TRIMDAC_CH86(4)	TRIMDAC_CH118(4)
bit 20	TRIMDAC_CH20(4)	TRIMDAC_CH52(4)	TRIMDAC_CH84(4)	TRIMDAC_CH116(4)
bit 19	TRIMDAC_CH19(4)	TRIMDAC_CH51(4)	TRIMDAC_CH83(4)	TRIMDAC_CH115(4)
bit 18	TRIMDAC_CH17(4)	TRIMDAC_CH49(4)	TRIMDAC_CH81(4)	TRIMDAC_CH113(4)
bit 17	TRIMDAC_CH18(4)	TRIMDAC_CH50(4)	TRIMDAC_CH82(4)	TRIMDAC_CH114(4)
bit 16	TRIMDAC_CH16(4)	TRIMDAC_CH48(4)	TRIMDAC_CH80(4)	TRIMDAC_CH112(4)
bit 15	TRIMDAC_CH15(4)	TRIMDAC_CH47(4)	TRIMDAC_CH79(4)	TRIMDAC_CH111(4)
bit 14	TRIMDAC_CH13(4)	TRIMDAC_CH45(4)	TRIMDAC_CH77(4)	TRIMDAC_CH109(4)
bit 13	TRIMDAC_CH14(4)	TRIMDAC_CH46(4)	TRIMDAC_CH78(4)	TRIMDAC_CH110(4)
bit 12	TRIMDAC_CH12(4)	TRIMDAC_CH44(4)	TRIMDAC_CH76(4)	TRIMDAC_CH108(4)
bit 11	TRIMDAC_CH11(4)	TRIMDAC_CH43(4)	TRIMDAC_CH75(4)	TRIMDAC_CH107(4)
bit 10	TRIMDAC_CH9(4)	TRIMDAC_CH41(4)	TRIMDAC_CH73(4)	TRIMDAC_CH105(4)
bit 9	TRIMDAC_CH10(4)	TRIMDAC_CH42(4)	TRIMDAC_CH74(4)	TRIMDAC_CH106(4)
bit 8	TRIMDAC_CH8(4)	TRIMDAC_CH40(4)	TRIMDAC_CH72(4)	TRIMDAC_CH104(4)
bit 7	TRIMDAC_CH7(4)	TRIMDAC_CH39(4)	TRIMDAC_CH71(4)	TRIMDAC_CH103(4)
bit 6	TRIMDAC_CH5(4)	TRIMDAC_CH37(4)	TRIMDAC_CH69(4)	TRIMDAC_CH101(4)
bit 5	TRIMDAC_CH6(4)	TRIMDAC_CH38(4)	TRIMDAC_CH70(4)	TRIMDAC_CH102(4)
bit 4	TRIMDAC_CH4(4)	TRIMDAC_CH36(4)	TRIMDAC_CH68(4)	TRIMDAC_CH100(4)
bit 3	TRIMDAC_CH3(4)	TRIMDAC_CH35(4)	TRIMDAC_CH67(4)	TRIMDAC_CH99(4)
bit 2	TRIMDAC_CH1(4)	TRIMDAC_CH33(4)	TRIMDAC_CH65(4)	TRIMDAC_CH97(4)
bit 1	TRIMDAC_CH2(4)	TRIMDAC_CH34(4)	TRIMDAC_CH66(4)	TRIMDAC_CH98(4)
bit 0	TRIMDAC_CH0(4)	TRIMDAC_CH32(4)	TRIMDAC_CH64(4)	TRIMDAC_CH96(4)
SEUbit	CR35SEU	CR35SEU	CR35SEU	CR35SEU
Reset Value (hex)	00000000	00000000	00000000	00000000

Table 11.50: TrimDAC registers (32 to 35)

Register Name	TrimDAC36	TrimDAC37	TrimDAC38	TrimDAC39
ADDR	$64	$65	$66	$67
bit 31	TRIMDAC_CH159(4)	TRIMDAC_CH191(4)	TRIMDAC_CH223(4)	TRIMDAC_CH255(4)
bit 30	TRIMDAC_CH157(4)	TRIMDAC_CH189(4)	TRIMDAC_CH221(4)	TRIMDAC_CH253(4)
bit 29	TRIMDAC_CH158(4)	TRIMDAC_CH190(4)	TRIMDAC_CH222(4)	TRIMDAC_CH254(4)
bit 28	TRIMDAC_CH156(4)	TRIMDAC_CH188(4)	TRIMDAC_CH220(4)	TRIMDAC_CH252(4)
bit 27	TRIMDAC_CH155(4)	TRIMDAC_CH187(4)	TRIMDAC_CH219(4)	TRIMDAC_CH251(4)
bit 26	TRIMDAC_CH153(4)	TRIMDAC_CH185(4)	TRIMDAC_CH217(4)	TRIMDAC_CH249(4)
bit 25	TRIMDAC_CH154(4)	TRIMDAC_CH186(4)	TRIMDAC_CH218(4)	TRIMDAC_CH250(4)
bit 24	TRIMDAC_CH152(4)	TRIMDAC_CH184(4)	TRIMDAC_CH216(4)	TRIMDAC_CH248(4)
bit 23	TRIMDAC_CH151(4)	TRIMDAC_CH183(4)	TRIMDAC_CH215(4)	TRIMDAC_CH247(4)
bit 22	TRIMDAC_CH149(4)	TRIMDAC_CH181(4)	TRIMDAC_CH213(4)	TRIMDAC_CH245(4)
bit 21	TRIMDAC_CH150(4)	TRIMDAC_CH182(4)	TRIMDAC_CH214(4)	TRIMDAC_CH246(4)
bit 20	TRIMDAC_CH148(4)	TRIMDAC_CH180(4)	TRIMDAC_CH212(4)	TRIMDAC_CH244(4)
bit 19	TRIMDAC_CH147(4)	TRIMDAC_CH179(4)	TRIMDAC_CH211(4)	TRIMDAC_CH243(4)
bit 18	TRIMDAC_CH145(4)	TRIMDAC_CH177(4)	TRIMDAC_CH209(4)	TRIMDAC_CH241(4)
bit 17	TRIMDAC_CH146(4)	TRIMDAC_CH178(4)	TRIMDAC_CH210(4)	TRIMDAC_CH242(4)
bit 16	TRIMDAC_CH144(4)	TRIMDAC_CH176(4)	TRIMDAC_CH208(4)	TRIMDAC_CH240(4)
bit 15	TRIMDAC_CH143(4)	TRIMDAC_CH175(4)	TRIMDAC_CH207(4)	TRIMDAC_CH239(4)
bit 14	TRIMDAC_CH141(4)	TRIMDAC_CH173(4)	TRIMDAC_CH205(4)	TRIMDAC_CH237(4)
bit 13	TRIMDAC_CH142(4)	TRIMDAC_CH174(4)	TRIMDAC_CH206(4)	TRIMDAC_CH238(4)
bit 12	TRIMDAC_CH140(4)	TRIMDAC_CH172(4)	TRIMDAC_CH204(4)	TRIMDAC_CH236(4)
bit 11	TRIMDAC_CH139(4)	TRIMDAC_CH171(4)	TRIMDAC_CH203(4)	TRIMDAC_CH235(4)
bit 10	TRIMDAC_CH137(4)	TRIMDAC_CH169(4)	TRIMDAC_CH201(4)	TRIMDAC_CH233(4)
bit 9	TRIMDAC_CH138(4)	TRIMDAC_CH170(4)	TRIMDAC_CH202(4)	TRIMDAC_CH234(4)
bit 8	TRIMDAC_CH136(4)	TRIMDAC_CH168(4)	TRIMDAC_CH200(4)	TRIMDAC_CH232(4)
bit 7	TRIMDAC_CH135(4)	TRIMDAC_CH167(4)	TRIMDAC_CH199(4)	TRIMDAC_CH231(4)
bit 6	TRIMDAC_CH133(4)	TRIMDAC_CH165(4)	TRIMDAC_CH197(4)	TRIMDAC_CH229(4)
bit 5	TRIMDAC_CH134(4)	TRIMDAC_CH166(4)	TRIMDAC_CH198(4)	TRIMDAC_CH230(4)
bit 4	TRIMDAC_CH132(4)	TRIMDAC_CH164(4)	TRIMDAC_CH196(4)	TRIMDAC_CH228(4)
bit 3	TRIMDAC_CH131(4)	TRIMDAC_CH163(4)	TRIMDAC_CH195(4)	TRIMDAC_CH227(4)
bit 2	TRIMDAC_CH129(4)	TRIMDAC_CH161(4)	TRIMDAC_CH193(4)	TRIMDAC_CH225(4)
bit 1	TRIMDAC_CH130(4)	TRIMDAC_CH162(4)	TRIMDAC_CH194(4)	TRIMDAC_CH226(4)
bit 0	TRIMDAC_CH128(4)	TRIMDAC_CH160(4)	TRIMDAC_CH192(4)	TRIMDAC_CH224(4)
SEUbit	CR39SEU	CR39SEU	CR39SEU	CR39SEU
Reset Value (hex)	00000000	00000000	00000000	00000000

Table 11.51: TrimDAC registers (36 to 39)

Register Name	CalREG0	CalREG1	CalREG2	CalREG3
ADDR	$68	$69	$6A	$6B
bit 31	CALENABLE_CH31	CALENABLE_CH63	CALENABLE_CH95	CALENABLE_CH127
bit 30	CALENABLE_CH29	CALENABLE_CH61	CALENABLE_CH93	CALENABLE_CH125
bit 29	CALENABLE_CH30	CALENABLE_CH62	CALENABLE_CH94	CALENABLE_CH126
bit 28	CALENABLE_CH28	CALENABLE_CH60	CALENABLE_CH92	CALENABLE_CH124
bit 27	CALENABLE_CH27	CALENABLE_CH59	CALENABLE_CH91	CALENABLE_CH123
bit 26	CALENABLE_CH25	CALENABLE_CH57	CALENABLE_CH89	CALENABLE_CH121
bit 25	CALENABLE_CH26	CALENABLE_CH58	CALENABLE_CH90	CALENABLE_CH122
bit 24	CALENABLE_CH24	CALENABLE_CH56	CALENABLE_CH88	CALENABLE_CH120
bit 23	CALENABLE_CH23	CALENABLE_CH55	CALENABLE_CH87	CALENABLE_CH119
bit 22	CALENABLE_CH21	CALENABLE_CH53	CALENABLE_CH85	CALENABLE_CH117
bit 21	CALENABLE_CH22	CALENABLE_CH54	CALENABLE_CH86	CALENABLE_CH118
bit 20	CALENABLE_CH20	CALENABLE_CH52	CALENABLE_CH84	CALENABLE_CH116
bit 19	CALENABLE_CH19	CALENABLE_CH51	CALENABLE_CH83	CALENABLE_CH115
bit 18	CALENABLE_CH17	CALENABLE_CH49	CALENABLE_CH81	CALENABLE_CH113
bit 17	CALENABLE_CH18	CALENABLE_CH50	CALENABLE_CH82	CALENABLE_CH114
bit 16	CALENABLE_CH16	CALENABLE_CH48	CALENABLE_CH80	CALENABLE_CH112
bit 15	CALENABLE_CH15	CALENABLE_CH47	CALENABLE_CH79	CALENABLE_CH111
bit 14	CALENABLE_CH13	CALENABLE_CH45	CALENABLE_CH77	CALENABLE_CH109
bit 13	CALENABLE_CH14	CALENABLE_CH46	CALENABLE_CH78	CALENABLE_CH110
bit 12	CALENABLE_CH12	CALENABLE_CH44	CALENABLE_CH76	CALENABLE_CH108
bit 11	CALENABLE_CH11	CALENABLE_CH43	CALENABLE_CH75	CALENABLE_CH107
bit 10	CALENABLE_CH9	CALENABLE_CH41	CALENABLE_CH73	CALENABLE_CH105
bit 9	CALENABLE_CH10	CALENABLE_CH42	CALENABLE_CH74	CALENABLE_CH106
bit 8	CALENABLE_CH8	CALENABLE_CH40	CALENABLE_CH72	CALENABLE_CH104
bit 7	CALENABLE_CH7	CALENABLE_CH39	CALENABLE_CH71	CALENABLE_CH103
bit 6	CALENABLE_CH5	CALENABLE_CH37	CALENABLE_CH69	CALENABLE_CH101
bit 5	CALENABLE_CH6	CALENABLE_CH38	CALENABLE_CH70	CALENABLE_CH102
bit 4	CALENABLE_CH4	CALENABLE_CH36	CALENABLE_CH68	CALENABLE_CH100
bit 3	CALENABLE_CH3	CALENABLE_CH35	CALENABLE_CH67	CALENABLE_CH99
bit 2	CALENABLE_CH1	CALENABLE_CH33	CALENABLE_CH65	CALENABLE_CH97
bit 1	CALENABLE_CH2	CALENABLE_CH34	CALENABLE_CH66	CALENABLE_CH98
bit 0	CALENABLE_CH0	CALENABLE_CH32	CALENABLE_CH64	CALENABLE_CH96
SEUbit	CR43SEU	CR43SEU	CR43SEU	CR43SEU
Reset Value (hex)	00000000	00000000	00000000	00000000

Table 11.52: Calibration Enable registers (0 to 3)

Register Name	CalREG4	CalREG5	CalREG6	CalREG7
ADDR	$6C	$6D	$6E	$6F
bit 31	CALENABLE_CH159	CALENABLE_CH191	CALENABLE_CH223	CALENABLE_CH255
bit 30	CALENABLE_CH157	CALENABLE_CH189	CALENABLE_CH221	CALENABLE_CH253
bit 29	CALENABLE_CH158	CALENABLE_CH190	CALENABLE_CH222	CALENABLE_CH254
bit 28	CALENABLE_CH156	CALENABLE_CH188	CALENABLE_CH220	CALENABLE_CH252
bit 27	CALENABLE_CH155	CALENABLE_CH187	CALENABLE_CH219	CALENABLE_CH251
bit 26	CALENABLE_CH153	CALENABLE_CH185	CALENABLE_CH217	CALENABLE_CH249
bit 25	CALENABLE_CH154	CALENABLE_CH186	CALENABLE_CH218	CALENABLE_CH250
bit 24	CALENABLE_CH152	CALENABLE_CH184	CALENABLE_CH216	CALENABLE_CH248
bit 23	CALENABLE_CH151	CALENABLE_CH183	CALENABLE_CH215	CALENABLE_CH247
bit 22	CALENABLE_CH149	CALENABLE_CH181	CALENABLE_CH213	CALENABLE_CH245
bit 21	CALENABLE_CH150	CALENABLE_CH182	CALENABLE_CH214	CALENABLE_CH246
bit 20	CALENABLE_CH148	CALENABLE_CH180	CALENABLE_CH212	CALENABLE_CH244
bit 19	CALENABLE_CH147	CALENABLE_CH179	CALENABLE_CH211	CALENABLE_CH243
bit 18	CALENABLE_CH145	CALENABLE_CH177	CALENABLE_CH209	CALENABLE_CH241
bit 17	CALENABLE_CH146	CALENABLE_CH178	CALENABLE_CH210	CALENABLE_CH242
bit 16	CALENABLE_CH144	CALENABLE_CH176	CALENABLE_CH208	CALENABLE_CH240
bit 15	CALENABLE_CH143	CALENABLE_CH175	CALENABLE_CH207	CALENABLE_CH239
bit 14	CALENABLE_CH141	CALENABLE_CH173	CALENABLE_CH205	CALENABLE_CH237
bit 13	CALENABLE_CH142	CALENABLE_CH174	CALENABLE_CH206	CALENABLE_CH238
bit 12	CALENABLE_CH140	CALENABLE_CH172	CALENABLE_CH204	CALENABLE_CH236
bit 11	CALENABLE_CH139	CALENABLE_CH171	CALENABLE_CH203	CALENABLE_CH235
bit 10	CALENABLE_CH137	CALENABLE_CH169	CALENABLE_CH201	CALENABLE_CH233
bit 9	CALENABLE_CH138	CALENABLE_CH170	CALENABLE_CH202	CALENABLE_CH234
bit 8	CALENABLE_CH136	CALENABLE_CH168	CALENABLE_CH200	CALENABLE_CH232
bit 7	CALENABLE_CH135	CALENABLE_CH167	CALENABLE_CH199	CALENABLE_CH231
bit 6	CALENABLE_CH133	CALENABLE_CH165	CALENABLE_CH197	CALENABLE_CH229
bit 5	CALENABLE_CH134	CALENABLE_CH166	CALENABLE_CH198	CALENABLE_CH230
bit 4	CALENABLE_CH132	CALENABLE_CH164	CALENABLE_CH196	CALENABLE_CH228
bit 3	CALENABLE_CH131	CALENABLE_CH163	CALENABLE_CH195	CALENABLE_CH227
bit 2	CALENABLE_CH129	CALENABLE_CH161	CALENABLE_CH193	CALENABLE_CH225
bit 1	CALENABLE_CH130	CALENABLE_CH162	CALENABLE_CH194	CALENABLE_CH226
bit 0	CALENABLE_CH128	CALENABLE_CH160	CALENABLE_CH192	CALENABLE_CH224
SEUbit	CR47SEU	CR47SEU	CR47SEU	CR47SEU
Reset Value (hex)	00000000	00000000	00000000	00000000

Table 11.53: Calibration Enable registers (4 to 7)

	HitCountREG0-63
	'h80 to 'hBF
bit 31	HitCount(7) CH3:mod4
bit 30	HitCount(6) CH3:mod4
bit 29	HitCount(5) CH3:mod4
bit 28	HitCount(4) CH3:mod4
bit 27	HitCount(3) CH3:mod4
bit 26	HitCount(2) CH3:mod4
bit 25	HitCount(1) CH3:mod4
bit 24	HitCount(0) CH3:mod4
bit 23	HitCount(7) CH2:mod4
bit 22	HitCount(6) CH2:mod4
bit 21	HitCount(5) CH2:mod4
bit 20	HitCount(4) CH2:mod4
bit 19	HitCount(3) CH2:mod4
bit 18	HitCount(2) CH2:mod4
bit 17	HitCount(1) CH2:mod4
bit 16	HitCount(0) CH2:mod4
bit 15	HitCount(7) CH1:mod4
bit 14	HitCount(6) CH1:mod4
bit 13	HitCount(5) CH1:mod4
bit 12	HitCount(4) CH1:mod4
bit 11	HitCount(3) CH1:mod4
bit 10	HitCount(2) CH1:mod4
bit 9	HitCount(1) CH1:mod4
bit 8	HitCount(0) CH1:mod4
bit 7	HitCount(7) CH0:mod4
bit 6	HitCount(6) CH0:mod4
bit 5	HitCount(5) CH0:mod4
bit 4	HitCount(4) CH0:mod4
bit 3	HitCount(3) CH0:mod4
bit 2	HitCount(2) CH0:mod4
bit 1	HitCount(1) CH0:mod4
bit 0	HitCount(0) CH0:mod4
SEUbit	-
Reset Value	00000000

Table 11.54: Hit Counters REGISTERS

- SLVS drivers current at mid-range
- BC counter at $00
- Register Readout is enabled
- L0 buffer latency at $190 (400 BC or 10us)
- Detection mode 00
- CF packet disabled
- No packet number limit
- After power up reset is released, High Priority Register packets are periodically transmitted until a valid command is received to stop the transmission.

11.19 E-FUSE option

24 eFuse bits are at disposition for individual chip marking. The Fuse programming has to be done during wafer probing as the using pads will not be bounded in the hybrid. Recommended sequence for programming:

- 1) Pull VFUSE from 1.5V (VDDD) to 3.3V (externally supplied)
- 2) Write the eFuse configuration register (and read back to control, both the decimal value and the register value2efuse in the status registers) (regular register commands)
- 3) Pull high (1.5V) FusePP_pad for 200us
- 4) Pull down FusePP_pad (0V)
- 5) Continue from 2 until all bits TO BE FUSED are done
- 6) Pull Vfuse down to 1.5V (VDDD)

It is recommended to fuse only one bit at a time: the register $25 should then be written with only 1 bit at one across the 32 bits.

Once programmed the fuse bits are read only with the status register at address $32.

Recommended sequence for reading:

- 1) Send command to write one at bit 5 of the SCreg ($00). This operation in needed to load the eFuse data into the Status Register $32.
- 2) Send command to read the eFuse Status Register (regular read register command, address $32)

The first step in needed only once after powerup or a RegReset command. Except when in programming, the Vfuse power input (at the back side) should be always connected to the external DVDD (1.5V). The FusePP_pad can be left floating in the hybrid. It has an internal pulldown that forces this input to ground if left floating.

11.20 Initialisation signatures

After powerup, application of clocks, there is the requirement that the ABCStar detects correctly the frame on the LCB_IN inputs which is a preliminary step necessary to get the capability to control the chip with the CMD bits and commands. A packet (HPR packet) is sent periodically (period of about 1ms) after a power-up after the first HPR, a Register_Reset or a hard RST_B signal. The packet contains the essential information concerning the LCB circuitry status, and the digital power voltage measured internally by the ADC. A specific control bit (StopHPR) in the configuration register $00 has to be set to one (hence requiring a correct function of the LCB circuits) to interrupt the periodic HPR packet transmission. HPR packets are also transmitted when the LCB link synchronization status changes (LCB_Locked). This can be disabled using the MaskHPR bit in Configuration Register $00. The HPR packet can be read through a regular read command at address $3F.

11.21 Programming Model

The various registers of the ABCStar ASIC should be programmed after powerup according to the register description in the functional description.

12 Radiation Tolerance and Other Special Requirements

The requirements for the accumulated ionizing dose are around 450 kGy(Si) for the inner barrel layer and 660 kGy(Si) for the endcap . The radiation tolerance will be measured up to 700kGy.

Various mitigation techniques are implemented in the design, to lower the occurrence of SEU bit flips, that may result in single or multiple bit errors (that can be accepted up to a certain point) or into functional interrupts (SEFI).

Below are given some expected values for bit error rates, that are projected from the current SEU error rates measurements done with the ABC130 ASIC.

The ABCStar chip should not experience any latchup in the LHC radiation environment.

12.1 Error rate in the L0Buffer

Calculations to estimate the probability of bit flip in the L0Buffer.

- Bit flip cross section : 5E-14/cm2 (CHARM measurements, June 2015)
- Particle hit rate in LHC environment at 5*10E34 (extrapolated from numbers at 1*10E34, pre H-LHC simulations) : 5 times 1.2E13/cm2.year of run (only simulation safety factor applied), at 35 cm radius.
- One run year time (6 months run) 15E6 seconds
- Hit rate per second : 4.0E6/cm2.s
- Bit flip 2E-7 per second per bit
- In 12.8us : probability of bit flip per bit : 2.56E-12
- For 164Kbits memory : probability of one bit flip per 30.5 seconds per memory
- In 12.8us : probability of one bit flip within 164K : 42E-6

From these numbers it appears that the physics data bit error rate will be 1 bit error per 1525 seconds (1/40 reduction rate and 256 physics data bit over 320), ie per 1.5E9 packets transmitted (a bit error translates in a false cluster position or false hit bit).

Considering only the 8 BCID bits for event identification the rate is reduced to one bit flip per 4.88E4 seconds per chip, ie per 48.8E9 packets transmitted (a BCID bit error translates into a false packet-to-event identification).

12.2 Error rate in the EvtBuffer

Calculations to estimate the probability of bit flip in the EvtBuffer.

- Bit flip cross section : 5E-14/cm2 (CHARM measurements, June 2015)
- Particle hit rate in LHC environment at 5*10E34 (extrapolated from numbers at 1*10E34, pre H-LHC simulations) : 5 times 1.2E13/cm2.year of run (only simulation safety factor applied), at 35 cm radius.
- One run year time (6 months run) 15E6 seconds
- Hit rate per second : 4.0E6/cm2.s
- Bit flip 2E-7 per second per bit
- In 128us : probability of bit flip per bit : 2.56E-11
- For 41Kbits memory : probability of one bit flip per 122 seconds per memory
- In 128us : probability of one bit flip within 41K : 1.05E-6
- From these numbers it appears that the physics data bit error rate will be 1 bit error per 152 seconds, (256 physics data bit over 320) ie per 152M packets transmitted (a bit error translates in a false cluster position or false hit bit).
- Considering only the 15 bits for event identification (L0tag and BCID) the rate is reduced to one bit flip per 2604 seconds, ie per 2.60E9 packets transmitted (a ID bit error translates into a false packet-to-event identification).

13 Testing, Validation and Commissioning

Describe testing procedures that will be used to demonstrate that the fabricated component meets the specifications. This should include radiation testing if radiation tolerance is one of the requirements. It is not required to complete this section prior to the first specification review but it should be completed prior to the PDR. Prior to the FDR, the production testing must be described, and prior to the PRR, commissioning plans must be included.

14 Reliability Matters

14.1 Consequences of Failures

A failure of ABCStar chip will cause the loss of ability to process the signals from 256 strips from the sensor.

14.1.1 Prior Knowledge of Expected Reliability

The ABCStar design is following the GF CMOS 8RF technology design rules, as described in the design guide lines documents. The design rules, and the recommendations to interpret them in particular cases, are given for the expected lifetime (run time) of 100K hours of operation at 100C. Formulations are given to predict the electromigration that affect metal tracks, degradations of transistors due to the hot carriers' effect, and possible VTh variations that may occur during the components lifetime. These three degradations effects are covered by predictive data or models in the documentation. In the literature one can find that the effects of accelerated degradation due to hot carriers starts below 200K. The GF CMOS 8RF technology process has been specified for -55C to +125C junction temperature. For the ABCStar ASIC application we should not see this effect. Burn-in tests of the devices (140 degrees, voltage overdrive) are suggested by the foundry, to cure the infant mortality losses. In our case we don't consider these tests at the component level. Our chips are operational in controlled environment, at moderate or low temperature, stabilized power, most of the time immune to electrical or thermal chocks. Essentially because of the low temperature and the controlled voltages, a large safety factor is gained in comparison to the estimations of life time limits due to the above effects. The hybrid burn-in will not affect directly the ABCStar, but the module assembly. Well known degradation effects due to the important radiation field are specific to our environment and are well documented for this technology with similar designs.

14.2 Measures Proposed to Insure Reliability of Component and/or System

Most of the digital ABCStar logic has been triplicated to mitigate the effects of SEU, including the decoding of the RESET commands. Spacing of the triplicated registers (minimum 10 um) has also been taken into account. The use of thick oxide capacitors instead of thin oxide capacitors for the decoupling, although having less capacitance per um2, should improve reliability and leakage. The analog frontend uses enclosed-layout transistors to improve the 1/f noise that increases with radiation.

14.3 Quality Assurance to Validate Reliability of Design and Construction or Manufacturing Techniques

A statistically significant samples of ABCStar ASICs will be tested under adverse environmental conditions, including irradiation and accelerated ageing, to demonstrate their reliability. Tests well beyond the expected temperature and radiation ranges are foreseen.

14.4 12.5 Quality Control to Validate Reliability Specifications during Production

Describe what stress tests will be applied during production, possibly on a sampling basis, to validate the reliability of production units. These could likely be destructive tests. Specify the required sampling percentage of production units. It is not required to complete this section prior to the first specification

review but it must be completed prior to the FDR. It is strongly recommended that these plans be reviewed and approved prior to the actual FDR to avoid the possibility of failing the FDR and thus delaying the fabrication or construction of the pre-production parts,

References

[1] "ATLAS ITk Electronics Specification: HCCStar", EDMS AT2-IS-CD-0003, https://edms.cern.ch/document/AT2-IS-CD-0003

[2] "ATLAS ITk Electronics Specification: AMAC", EDMS AT2-IS-CD-0004, https://edms.cern.ch/document/AT2-IS-CD-0004

[3] "ATLAS ITk Electronics Specification: Bus Tape", EDMS AT2-IS-ES-0006, https://edms.cern.ch/document/AT2-IS-ES-0006

[4] "ATLAS ITk Electronics Specification: EOS", EDMS AT2-IS-ES-0003, https://edms.cern.ch/document/AT2-IS-ES-0003

[5] "ATLAS ITk Electronics Specification: Hybrid", EDMS AT2-IS-CD-0005, https://edms.cern.ch/document/AT2-IS-CD-0005

[6] "ATLAS ITk Electronics Specification: Module", EDMS AT2-IS-CD-0006, https://edms.cern.ch/document/AT2-IS-CD-0006

[7] "ATLAS ITk Electronics Specification: Power Board", EDMS AT2-IS-CD-0007, https://edms.cern.ch/document/AT2-IS-CD-0007

[8] ATLAS ITk Strips TDR

A Appendix. ABCS front end model for SPICE simulation

```
// Generated for: spectre
// Generated on: Aug 30 12:11:13 2016
// Design library name: ABCFEMODEL
// Design cell name: ABCStarChannel
// Design view name: schematic
simulator lang=spectre
global 0
//VT: threshold in mV
parameters VT
include "allModels.scs" section=tt
include "design.scs"
// Library name: ABCFEMODEL
// Cell name: ABCStarChannel
// View name: schematic
V16 (net42 0) vsource dc=VT-7.33m type=dc
R18 (0 net18) resistor r=1M
R22 (net25 net26) resistor r=10K c=0
R19 (0 CASOUT) resistor r=1.75M
R20 (0 net17) resistor r=1M
R17 (POUT net33) resistor r=6K
R29 (net41 net29) resistor r=10K c=0
R21 (POUT IN) resistor r=100K
R32 (0 net28) resistor r=500K c=0
R34 (0 net24) resistor r=400K
R37 (POUT net22) resistor r=15K c=0
R36 (net22 net25) resistor r=150K c=0
R31 (net26 SHOUT) resistor r=10K c=0
G6 (net18 0 net17 0) vccs gm=-1u type=vccs inputtype=single max=10m
G1 (net24 0 net22 0) vccs gm=1m type=vccs inputtype=single max=10m
G5 (net17 0 CASOUT 0) vccs gm=-1u type=vccs inputtype=single max=10m
G7 (CASOUT 0 IN 0) vccs gm=4.2m type=vccs inputtype=single max=10m
E2 (ANOUT 0 net29 net42) vcvs gain=1 type=vcvs max=800m
E0 (net41 0 net28 0) vcvs gain=-3.8 type=vcvs
E4 (net25 0 net24 0) vcvs gain=1.0 type=vcvs max=10 abs=off
E5 (net33 0 net18 0) vcvs gain=1.0 type=vcvs max=10 abs=off
E6 (DIGOUT 0 ANOUT 0) vcvs gain=10000 td=6n type=vcvs min=0 max=1.2
E3 (net38 0 SHOUT 0) vcvs gain=1 type=vcvs
C38 (net26 0) capacitor c=400.0f
C67 (SHOUT 0) capacitor c=400.0f
C30 (net17 0) capacitor c=250.00a
C31 (CASOUT 0) capacitor c=25f
C35 (IN CASOUT) capacitor c=60f
C69 (net29 0) capacitor c=400.0f
C32 (net18 0) capacitor c=250.00a
C34 (IN POUT) capacitor c=60f
C40 (POUT 0) capacitor c=20f
C68 (net38 net28) capacitor c=500.0f
C71 (net24 0) capacitor c=180f
simulatorOptions options reltol=1e-3 vabstol=1e-6 iabstol=1e-12 temp=27 \
    tnom=25 scalem=1.0 scale=1.0 gmin=1e-12 rforce=1 maxnotes=5 maxwarns=5 \
    digits=5 cols=80 pivrel=1e-3 sensfile="../psf/sens.output" \
    checklimitdest=psf
modelParameter info what=models where=rawfile
element info what=inst where=rawfile
outputParameter info what=output where=rawfile
designParamVals info what=parameters where=rawfile
```

```
primitives info what=primitives where=rawfile
subckts info what=subckts where=rawfile
saveOptions options save=allpub
```

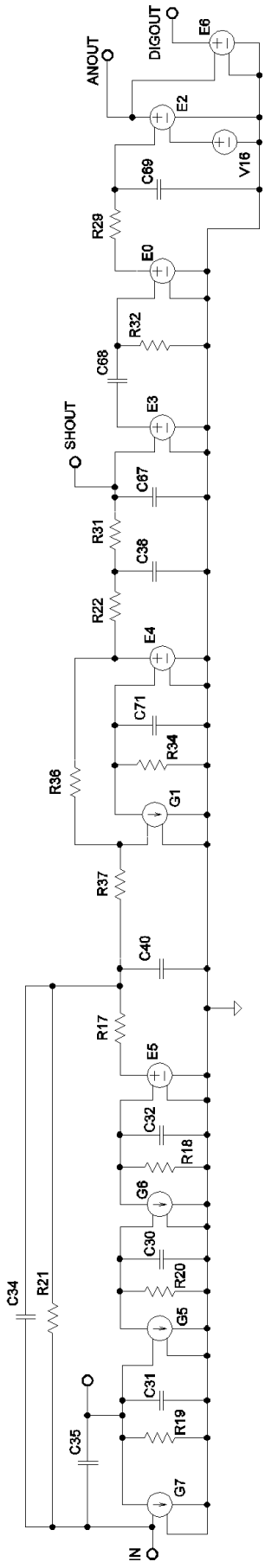

Figure A.1: Front-end Model schematic

B Appendix. Front-end validation

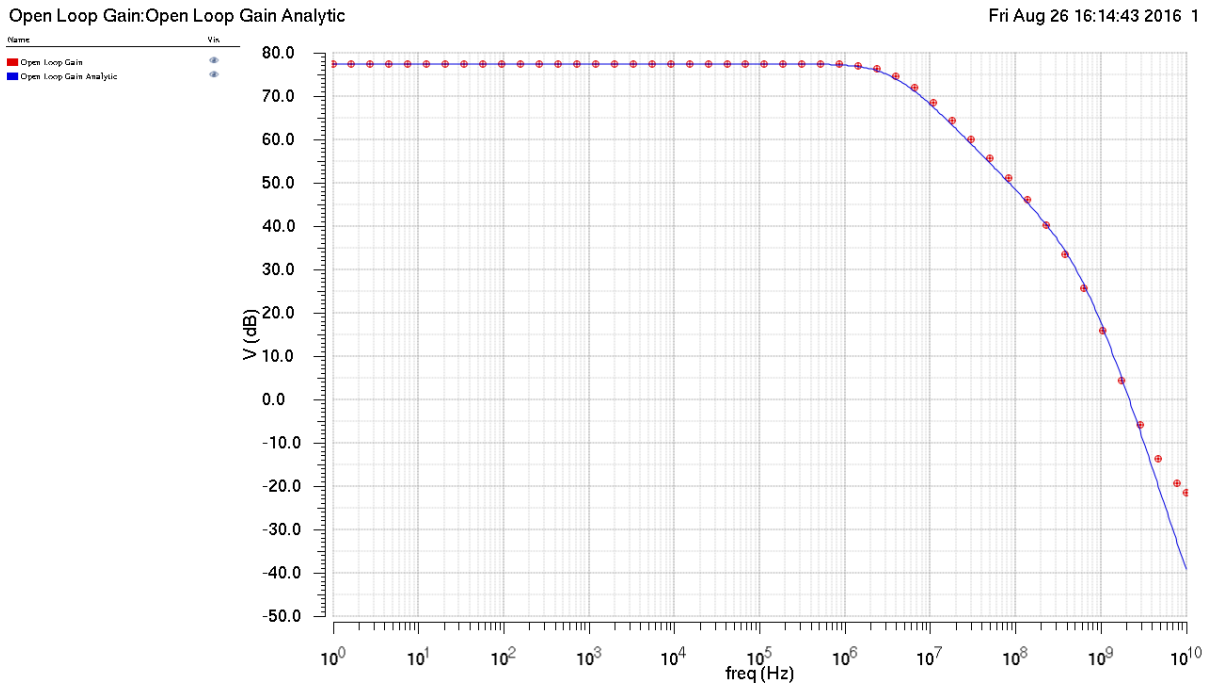

Figure B.1: Preamplifier open loop gain: simplified model (blue trace) and full schematic (red data points)

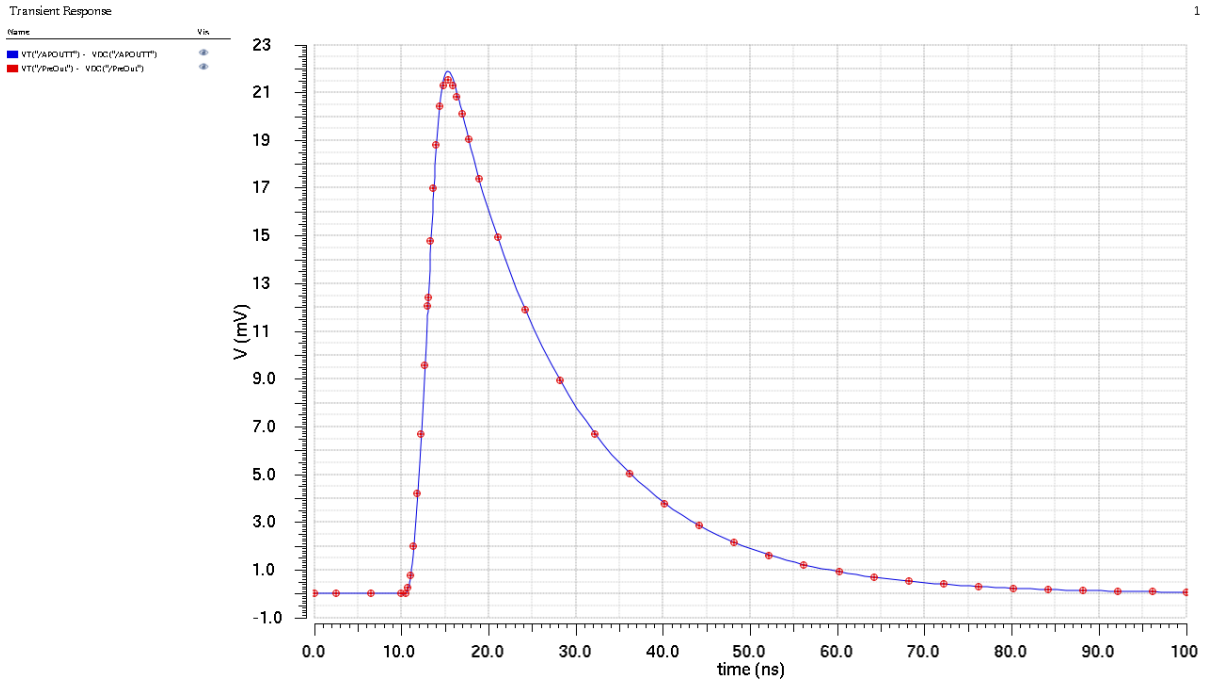

Figure B.2: Preamplifier response to -3.5fC (Cin=5pF): simplified model (blue trace) and full schematic (red data points)

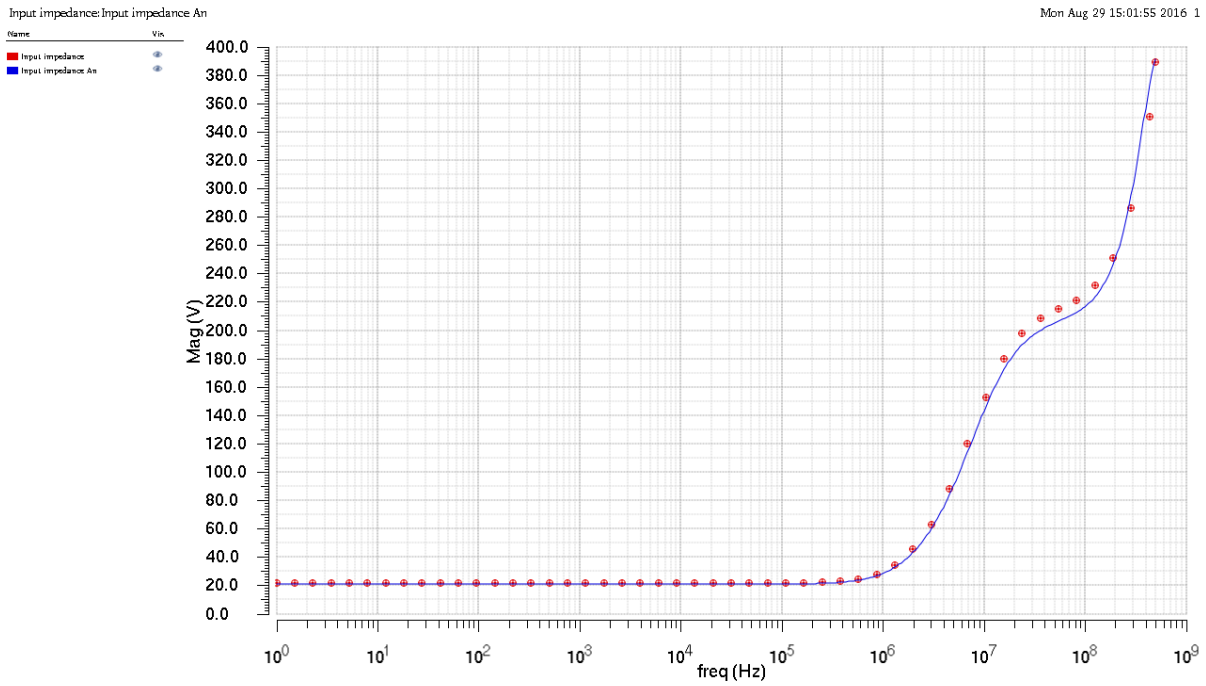

Figure B.3: Preamplifier input impedance: simplified model (blue trace) and full schematic (red data points)

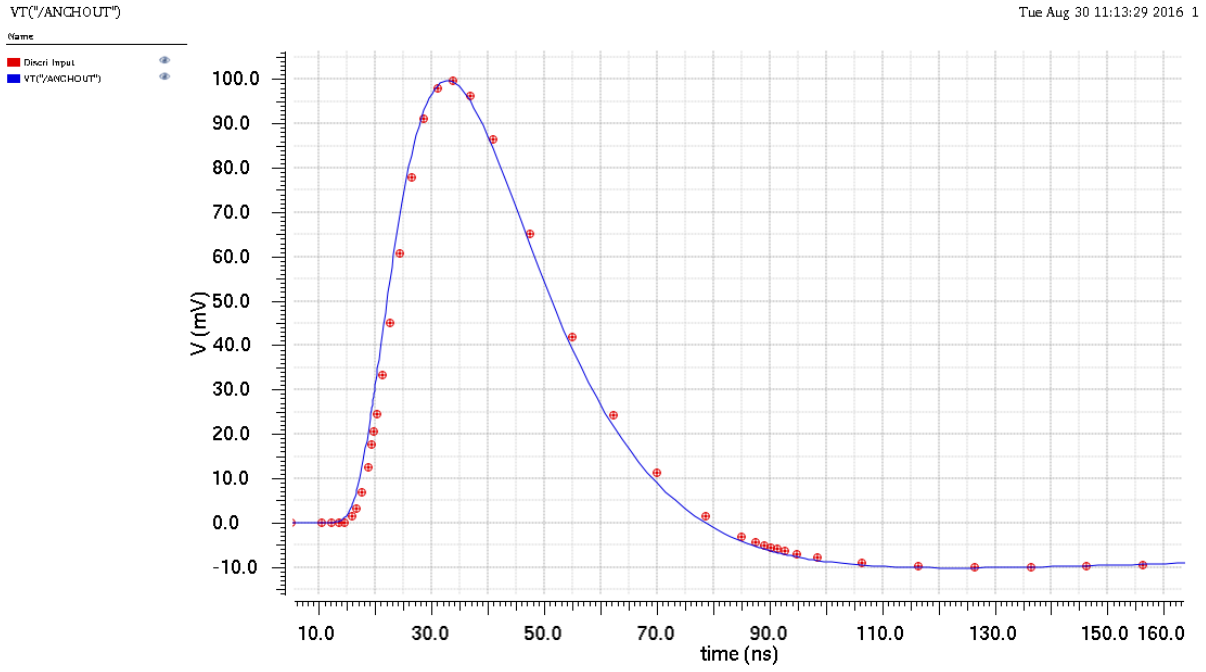

Figure B.4: Full chain response to -1fC signal (as seen at discriminator input): simplified model (blue trace) and full schematic (red data points)

C Appendix. Detailed pinout list

	rate (MHz)	direction	Type		DC	ESD model	Functional device	Resistor

//from the detector (front)								
AIN[255:0]	40	I	Analogue	Inputs to FE channels		FE_PAD_SOFICS (lib:SCT2016) : 2x SOFICS 1kV HBM VDD_A/GND_A		22 Ohm
//Left side signals								
DVSS		Power	ESD Return	0V Ground specific to ESD return	0V	AGIO_DVSS : antiparallel diodes DVSS/GND		
VFUSE		Power	Efuse Power	To VDD raw on hybrid	3.3/1.5V	AGIO_DVDD_efuse : 3.3V RC power clamp DVDD/DVSS		
FusePP_pad		I	CMOS Pull-Down	To efuse units	0V	PIOSFC_INP_PD : 2x SOFICS 1kV HBM DVDD/DVSS	CMOS buffer on reg. VDDD	50 Ohm
//"Back" side signals								
DVSS		Power	ESD Return	0V Ground specific to ESD return	0V	AGIO_DVSS : antiparallel diodes DVSS/GND		
VFUSE		Power	Efuse Power	To VDD raw on hybrid	3.3/1.5V	AGIO_DVDD_efuse : 3.3V RC power clamp DVDD/DVSS		
BC_padN	40	I	SLVS	40MHz clock input		PIOSFC_ANA_50 : 2x SOFICS 1kV HBM DVDD/DVSS	LVDS receiver	50 Ohm
BC_padP	40	I	SLVS	40MHz clock input		PIOSFC_ANA_50 : 2x SOFICS 1kV HBM DVDD/DVSS	LVDS receiver	50 Ohm
DVSS		Power	ESD Return	0V Ground specific to ESD return	0V	AGIO_DVSS : antiparallel diodes DVSS/GND		
PRLP_padN	40 DDR	I	SLVS	Multiplexed PR LP input (80Mb/s)		PIOSFC_ANA_50 : 2x SOFICS 1kV HBM DVDD/DVSS	LVDS receiver	50 Ohm

PRLP_padP	40 DDR	I	SLVS	Multiplexed PR LP input (80Mb/s)		PIOSFC_ANA_50 : 2x SOFICS 1kV HBM DVDD/D-VSS	LVDS receiver	50 Ohm
GNDD		Power	Digital Ground	0V Digital Ground	0V	AGIO_GND : antiparallel diodes GND/D-VSS		
RSTB_Pad	Static	I	CMOS Pull-Up	External Hard Reset signal	1.5V	PIOSFC_INP : 2x SOFICS 1kV HBM DVDD/D-VSS	CMOS buffer on reg. VDDD	50 Ohm
PowerLow_pad	Static	I	CMOS Pull-Down	Low Power mode when at one	0	PIOSFC_INP_RAW_PD : 2x SOFICS 1kV HBM DVDD/D-VSS	CMOS buffer on raw VDD	50 Ohm
GNDD		Power	Digital Ground	0V Digital Ground	0V	AGIO_GND : antiparallel diodes GND/D-VSS		
padShuntCtrl	Analogue	I	Analogue	Shunt Device Control (analogue signal)		DGNFETProt_Res50_Pad : Unsiliced NFET, 50ohms, DVSS	Analogue	50 Ohm
GNDD		Power	Digital Ground	0V Digital Ground	0V	AGIO_GND : antiparallel diodes GND/D-VSS		
DVDD		Power	Ext. Digital Power	Ext. Power for Digital	1.5V	AGIO_DVDD : 3.3V RC power clamp DVDD/D-VSS		
VDDD		Power	Reg. Digital Power	Regulated Power for Digital	1.2V	AGIO_VDD : 1.2V RC power clamp VDD/GND		
GNDD		Power	Digital Ground	0V Digital Ground	0V	AGIO_GND : antiparallel diodes GND/D-VSS		
DVDD		Power	Ext. Digital Power	Ext. Power for Digital	1.5V	AGIO_DVDD : 3.3V RC power clamp DVDD/D-VSS		

VDDD		Power	Reg. Digital Power	Regulated Power for Digital	1.2V	AGIO_VDD : 1.2V RC power clamp VDD/GND		
GNDD		Power	Digital Ground	0V Digital Ground	0V	AGIO_GND : antiparallel diodes GND/DVSS		
DVDD		Power	Ext. Digital Power	Ext. Power for Digital	1.5V	AGIO_DVDD : 3.3V RC power clamp DVDD/DVSS		
VDDD		Power	Reg. Digital Power	Regulated Power for Digital	1.2V	AGIO_VDD : 1.2V RC power clamp VDD/GND		
DVSS		Power	ESD Return	0V Ground specific to ESD return	0V	AGIO_DVSS : antiparallel diodes DVSS/GND		
AVSS		Power	ESD Return	0V Ground specific to ESD return	0V	AGIO_DVSS : antiparallel diodes DVSS/GND A		
GNDIT		Power	Analogue Ground	0V Analogue Ground to FE branch	0V	PAD_GNDIT : antiparallel diodes GNDIT/DVSS A		
VDDA		Power	Reg. Analogue Power	Regulated Power for Analogue	1.2V	AGIO_VDD : 1.2V RC power clamp VDD/GND A		
GNDA		Power	Analogue Ground	0V Analogue Ground	0V	AGIO_GND : antiparallel diodes GND/DVSS A		
AVDD		Power	Ext. Analogue Power	Ext. Power for Analogue	1.5V	AGIO_DVDD : 3.3V RC power clamp DVDD/DVSS A		
GNDIT		Power	Analogue Ground	0V Analogue Ground to FE branch	0V	PAD_GNDIT : antiparallel diodes GNDIT/DVSS A		

VDDA		Power	Reg. Analogue Power	Regulated Power for Analogue	1.2V	AGIO_VDD : 1.2V RC power clamp VDD/GND A		
GNDA		Power	Analogue Ground	0V Analogue Ground	0V	AGIO_GND : antiparallel diodes GND/DVSS		
AVDD		Power	Ext. Analogue Power	Ext. Power for Analogue	1.5V	AGIO_DVDD : 3.3V RC power clamp DVDD/DVSS A		
GNDIT		Power	Analogue Ground	0V Analogue Ground to FE branch	0V	PAD_GNDIT : antiparallel diodes GNDIT/DVSS A		
VDDA		Power	Reg. Analogue Power	Regulated Power for Analogue	1.2V	AGIO_VDD : 1.2V RC power clamp VDD/GND A		
GNDA		Power	Analogue Ground	0V Analogue Ground	0V	AGIO_GND : antiparallel diodes GND/DVSS		
AVDD		Power	Ext. Analogue Power	Ext. Power for Analogue	1.5V	AGIO_DVDD : 3.3V RC power clamp DVDD/DVSS A		
GNDIT		Power	Analogue Ground	0V Analogue Ground to FE branch	0V	PAD_GNDIT : antiparallel diodes GNDIT/DVSS A		
VDDA		Power	Reg. Analogue Power	Regulated Power for Analogue	1.2V	AGIO_VDD : 1.2V RC power clamp VDD/GND A		
GNDA		Power	Analogue Ground	0V Analogue Ground	0V	AGIO_GND : antiparallel diodes GND/DVSS		

AVDD		Power	Ext. Analogue Power	Ext. Power for Analogue	1.5V	AGIO_DVDD : 3.3V RC power clamp DVDD/DVSS A		
AVSS		Power	ESD Return	0V Ground specific to ESD return	0V	AGIO_DVSS : double diode breaker DVSS/GND A		
ADCAL		I	Analogue	ADC Calibration		SIOWIRE_ANA_SOFICS : 2x SOFICS ECR structures DVSS A		90 Ohm
GNDD		Power	Digital Ground	0V Digital Ground	0V	AGIO_GND : antiparallel diodes GND/DVSS		
DVDD		Power	Ext. Digital Power	Ext. Power for Digital	1.5V	AGIO_DVDD : 3.3V RC power clamp DVDD/DVSS		
VDDD		Power	Reg. Digital Power	Regulated Power for Digital	1.2V	AGIO_VDD : 1.2V RC power clamp VDD/GND		
GNDD		Power	Digital Ground	0V Digital Ground	0V	AGIO_GND : antiparallel diodes GND/DVSS		
DVDD		Power	Ext. Digital Power	Ext. Power for Digital	1.5V	AGIO_DVDD : 3.3V RC power clamp DVDD/DVSS		
VDDD		Power	Reg. Digital Power	Regulated Power for Digital	1.2V	AGIO_VDD : 1.2V RC power clamp VDD/GND		
padID(0:3)	Static	I	CMOS Pull-Up	Chip Address (4 pads)	1.5V	PIOSFC_INP : 2x SOFICS 1kV HBM DVDD/DVSS	CMOS buffer on reg. VDDD	50 Ohm
DVSS		Power	ESD Return	0V Ground specific to ESD return	0V	AGIO_DVSS : antiparallel diodes DVSS/GND		

LCB_IN_padN	160	I	SLVS	Encoded COM L0 BCR input (160Mb/s)		PIOSFC_ANA_50 : 2x SOFICS 1kV HBM DVDD/D-VSS	LVDS receiver	50 Ohm
LCB_IN_padP	160	I	SLVS	Encoded COM L0 BCR input (160Mb/s)		PIOSFC_ANA_50 : 2x SOFICS 1kV HBM DVDD/D-VSS	LVDS receiver	50 Ohm
GNDD		Power	Digital Ground	0V Digital Ground	0V	AGIO_GND : antiparallel diodes GND/D-VSS		
CLK_padN	160	I	SLVS	Readout rate clock input		PIOSFC_ANA_50 : 2x SOFICS 1kV HBM DVDD/D-VSS	LVDS receiver	50 Ohm
CLK_PadP	160	I	SLVS	Readout rate clock input		PIOSFC_ANA_50 : 2x SOFICS 1kV HBM DVDD/D-VSS	LVDS receiver	50 Ohm
DVSS		Power	ESD Return	0V Ground specific to ESD return	0V	AGIO_DVSS : antiparallel diodes DVSS/GND		
DAT	160	O	SLVS	DATA signal		PIOSFC_ANA : 2x SOFICS 1kV HBM DVDD/D-VSS	LVDS driver	0 Ohm
DATB	160	O	SLVS	DATA signal		PIOSFC_ANA : 2x SOFICS 1kV HBM DVDD/D-VSS	LVDS driver	0 Ohm
//Right side signals								
abcup_pad		I	CMOS Pull-Down	Reserved	0	PIOSFC_INP_PD : 2x SOFICS 1kV HBM DVDD/D-VSS	CMOS buffer on reg. VDDD	50 Ohm
VDDD		Power	Reg. Digital Power	Regulated Power for Digital	1.2V	AGIO_VDD : 1.2V RC power clamp VDD/GND		
SDO_BC	MHz	O	CMOS 8mA	Output for CLK Scan Path chain		SIOBPU08_B_output		

GNDD		Power	Digital Ground	0V Digital Ground	0V	AGIO_GND : antiparallel diodes GND/D-VSS		
SDI_BC	MHz	I	CMOS Pull-Down	Input for BC Scan Path chain	0	PIOSFC_INP_PD : 2x SOFICS 1kV HBM DVDD/D-VSS	CMOS buffer on reg. VDDD	50 Ohm
GNDD		Power	Digital Ground	0V Digital Ground	0V	AGIO_GND : antiparallel diodes GND/D-VSS		
SDO_CLK	MHz	O	CMOS 8mA	Output for CLK Scan Path chain		SIOBPU08_B_output		
GNDD		Power	Digital Ground	0V Digital Ground	0V	AGIO_GND : antiparallel diodes GND/D-VSS		
SDI_CLK	MHz	I	CMOS Pull-Down	Input for BC Scan Path chain	0	PIOSFC_INP_PD : 2x SOFICS 1kV HBM DVDD/D-VSS	CMOS buffer on reg. VDDD	50 Ohm
GNDD		Power	Digital Ground	0V Digital Ground	0V	AGIO_GND : antiparallel diodes GND/D-VSS		
Scan_Enable	Static	O	CMOS Pull-Down	Enable Scan Path chains	0	PIOSFC_INP_PD : 2x SOFICS 1kV HBM DVDD/D-VSS	CMOS buffer on reg. VDDD	50 Ohm
VDDD		Power	Reg. Digital Power	Regulated Power for Digital	1.2V	AGIO_VDD : 1.2V RC power clamp VDD/GND		
GNDD		Power	Digital Ground	0V Digital Ground	0V	AGIO_GND : antiparallel diodes GND/D-VSS		
padTESTCOM	Analogue	O	Analogue	Discriminator bias "spy" point		PIOSFC_ANA : 2x SOFICS 1kV HBM DVDD/D-VSS		50 Ohm

TESTRES	Analogue	I	Analogue	Reference resistance	R	ANA_PAD_SOFICS (lib:SCT2016) : 2x SOFICS 1kV HBM VDD_A/GND_A	90 Ohm
GNDA_local		Power	Analog Ground	0V Analogue Ground	0	VLOW_PAD (lib:SCT2016)	
AMUXOUT	Analogue	O	Analogue	Analogue "spy" output		ANA_PAD_SOFICS (lib:SCT2016) : 2x SOFICS 1kV HBM VDD_A/GND_A	90 Ohm